V07070
INSTRUMENT Sho.

INSTRUCTION MANUAL

MODEL 5130A
0.1—160 MHz
PHASE CONTINUOUS
FREQUENCY SYNTHESIZER

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SECTION 1

GENERAL INFORMATION

1-1. INTRODUCTION

The Wavetek Rockland Model 5130A Phase Continuous Frequency Synthesizer is a precision frequency generator. It uses the accuracy and stability of a reference frequency standard operating at 5.0 or 10.0 MHz, either built-in or external, to produce output frequencies between 100 KHz and 159.999999999 MHz, with 1 mHz resolution. All output frequencies are coherent with the reference standard frequency and reflect its stability and accuracy. Any frequency within the above band may be selected by manual control with 0.1 Hz resolution or by remote control with 1 mHz resolution. The leveled output is +3 to +13 dBm into 50 Ohms and may be adjusted manually by the front panel control or remotely by an external dc voltage.

The Model 5130A is a direct Frequency Synthesizer capable of providing signals for many uses requiring stable and accurate sinewave signals with low attendant spurious outputs, low phase noise and fast and phase continuous transfer between selected frequencies. Typical applications include communications, spectrum analysis and surveillance, radar and automatic test systems with both narrow and wide-band coverage.

1-2. DESCRIPTION

ELECTRICAL. Model 5130A operates from either 115 or 230 Vac, 47-400 Hz and consumes 75 Watts of power. A rear-panel line selector switch selects the nominal line voltage. The case of the instrument is grounded through the power cord.

Manual frequency selection is accomplished via eight 10 - position (0-9) and one 16 - position (0-15) continuous-rotation switches. The lowest recommended frequency setting is 0.100000 MHz. For frequency settings lower than this value, the output will not be leveled and harmonic distortion will increase. The RF output is available on the front panel, or, optionally, at the rear panel and 10 dB range in level adjustment is provided. Local or Remote operation is indicated by LED's.

Remote frequency selection is accomplished via two rear panel connectors for BCD programming or optionally through an IEEE Standard 488/1978 connector mounted on the rear panel.

MECHANICAL. The instrument cabinet is 5.25 inches high by 17 inches wide (19 inches wide including rack mounts). It is 19 inches deep behind the rack mounts and 20.75 inches deep overall. Weight is approximately 33 pounds.

The power switch and operating controls are located on the front panel. The rear panel contains the power connector, fuse holder, programming connector,

line selector switch and a selector switch, together with associated BNC connectors, for external/internal frequency standard.

In its standard configuration the instrument is supplied in a cabinet suitable for table-top use, or for rack-mounting.

1-3. OPTIONS

Model 5130A is furnished without an internal frequency standard for use with an external 5 MHz or 10 MHz frequency reference. The following internal standards are available at extra cost:

Option -01:	High - Stability Frequency Standard, $\pm 4 \times 10^{-9}$ /day.
Option -02:	TCXO Frequency Standard, $\pm 4 \times 10^{-6}$ /year.

In addition to the 5 MHz or 10 MHz external input reference, Option -07 permits using a 1 MHz Standard as an external reference.

The output signal is optionally available on the rear panel instead of the front panel at no extra cost (Option -03).

For remote programming of frequency and amplitude a built-in IEEE Standard 488/1978 (Option -06) is available in lieu of the BCD programming.

1-4. SPECIFICATIONS, MODEL 5130A

FREQUENCY

Range:	0.1 MHz to 159.999999999 MHz
Resolution:	0.1 Hz Local, 0.001 Hz Remote
Control:	Local by continuous-rotation switches. Remote by TTL, parallel entry BCD, negative-true logic; remote enable line for all digits, except .01 Hz and .001 Hz.

REMOTE PROGRAMMING CHARACTERISTICS

Switching Time:	5-20 microsec for any combination of frequencies.
Phase Continuity:	Phase continuity maintained between chosen switched frequencies using any combination of the 8 digits below 100 KHz.
Switching Spurious:	Spectral purity specification not degraded when switching frequency below

100 KHz band, using decades through 10 KHz. (Sweep rate should not exceed 20 KHz.)

SPURIOUS OUTPUTS

Non-Harmonic: 70 dB below fundamental, 0.1 MHz to 160 MHz. (Typically greater than 75 dB).

Harmonic: 35 dB below fundamental at full output, 1 MHz to 160 MHz. (Typically greater than 40 dB).

SIGNAL TO NOISE RATIO (TYPICAL)

Phase: Greater than 70 dB

Amplitude: Greater than 80 dB

Measured in a 30 KHz band excluding 1 Hz centered on the fundamental.

PHASE NOISE SPECTRAL DENSITY

Guaranteed SSB S/N ratio measured in 1 Hz bandwidth, also, see Fig. 1-1.

Offset Frequency	Guaranteed S/N
10 Hz	93 dB
100 Hz	100 dB
1 KHz	110 dB
10 KHz	115 dB
100 KHz	125 dB

OUTPUT

Level: Nominal level adjustable from +3 dBm to +13 dBm into 50 Ohms.

Flatness: ±0.5 dB, 0.1 MHz to 159.9999999 MHz at +13 dBm.

Control: Local by continuous adjustment. Remote by external dc voltage, 0.6 to 2.0 Volts typical range.

Settling Time: 50 microsec

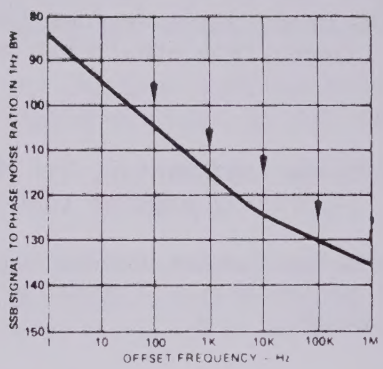


Fig. 1-1. Typical phase-noise performance. Guaranteed points are also indicated.

OPTIONAL FREQUENCY STANDARDS

Frequency: 10.000 MHz

Option	Aging Rate	Temperature Stability
-01	$\pm 4 \times 10^{-9}$ /day	$\pm 1 \times 10^{-8}$, 0°C to 40°C
-02	$\pm 4 \times 10^{-6}$ /year	$\pm 1 \times 10^{-6}$, 0°C to 40°C

AUXILIARY OUTPUT	10.000 MHz, 0.4 V rms into 50 Ohms, nominal.
REFERENCE INPUT	5.000 or 10.000 MHz, 0.4 V rms into 300 Ohms, nominal, or optional 1 MHz 0.4 V rms into 50 Ohms, nominal
POWER REQUIREMENTS	115/230 VAC ± 10%, 47-440 Hz, 75 W
OPERATING AMBIENT	0°C to 40°C
SIZE	5.25" H x 19" W x 19" D (13.3 cm x 48.3 cm x 48.3 cm) Mounts in standard RETMA rack.
WEIGHT	33 lbs. (15 Kg) net, approx. 40 lbs. (18 Kg) Shipping.

SECTION 2

OPERATION

2-1. INTRODUCTION

The instrument is electrically operational as shipped from the factory. The following paragraphs describe inspection, power requirements, installation and operation.

2-2. INSPECTION

This instrument was carefully inspected and tested prior to shipment. It was operated for a number of hours to reduce the probability of early failure. After unpacking the unit, inspect it carefully for shipping damage. Check especially for broken controls and connectors, dented or scratched cabinet parts. Should the instrument show any signs of damage, file a claim with the carrier immediately. Preserve the carton and packing materials; they will be required by the carrier.

It is recommended that conformance to specifications be verified upon receipt. In case of discrepancies, refer to the warranty at the beginning of this manual.

2-3. INSTALLATION AND POWER REQUIREMENTS

The 5130 Frequency Synthesizer is designed for table-top operation or installation in a standard 19 inch RETMA rack. Ambient temperature within the rack must not exceed +40°C while the instrument is operating. Where shock or vibration are encountered, it is suggested that additional support at the rear or sides of the instrument be provided. Other paragraphs in this section describe connections and switch settings which should be made before the unit is installed.

CAUTION
Always ensure that the 115/230 Volt switch is set for the nominal line voltage and that a fuse of the proper rating is installed in the instrument. If the switch is set incorrectly or a fuse of the wrong rating is used, the instrument may be damaged or fail to operate.

The instrument will operate from either 115 or 230 VAC, 47-440 Hz. Conversion for the line voltage is performed with a slide switch mounted on the rear panel. The unit is shipped with the switch set for 115 volts. To change the setting, insert a small-blade screwdriver in the switch slot and move switch to expose 115 for 115 VAC operation, or 230 for 230 VAC operation. The 2-Amp slow-blow fuse should be used for 115 VAC and the 1-Amp fuse should be used for 230 VAC operation.

WARNING
In keeping with standard safety practice, the case of the instrument is grounded through the power cord. If the instrument must be connected to a two-wire receptacle, use a parallel - ground adapter and connect the short lead to ground.

2-4. CONTROLS AND INDICATORS

Controls and indicators are shown in Fig. 2-1 and described in Table 2-1. The descriptions in Table 2-1 and the following paragraphs are not intended to be complete operating instructions, but only general information applying to different modes of operation.

Fig. 2-1b Model 5130A Controls
and Indicators

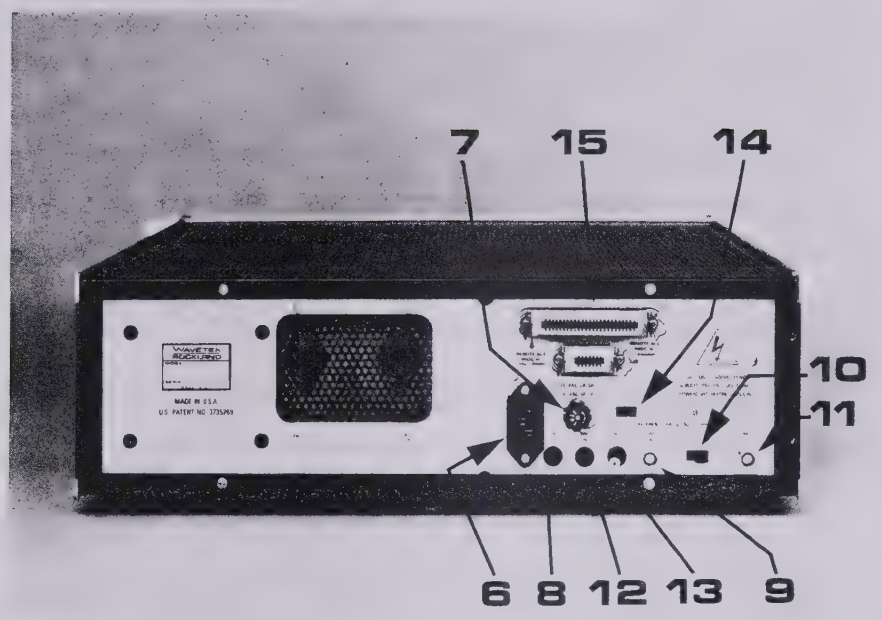
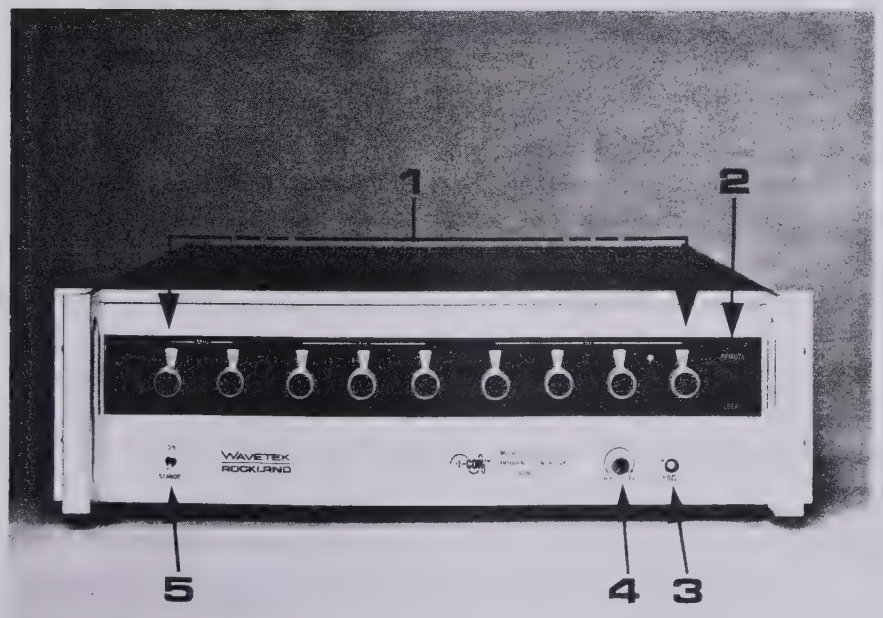


Fig. 2-1a Model 5130A Controls
and Indicators



NUMBER	DESCRIPTION
1	Frequency Selector Switches: A sixteen-position switch controls the 10 MHz steps and ten-position switches control the 1 MHz to 0.1 Hz steps. The highest output frequency obtainable is 159.9999999 MHz. The lowest recommended setting is 0.1000000 MHz.
2	Local/Remote Indicators: LED's indicate the mode in which the instrument is operated. The Remote mode is enabled via the program connector on the rear panel. Dial settings indicate output frequency only when operating in the Local Mode.
3	Output Connector: BNC jack supplies instrument signal output.
4	Level: Continuously variable control to set output to desired level between +3 and +13 dBm into 50 Ohms. (Nominal values).
5	Power Switch: Power is either full-on or applied to a few critical circuits in the standby mode.
6	Primary power receptacle, 3 wire. Accepts power cord supplied with instrument.
7	Fuse Holder: Fuse rating and primary supply voltage for the instrument are indicated above the fuse holder.
8	Optional location for instrument main output jack. If equipped, the front panel output connector is inactive.
9	External frequency standard input, accepts 5.000000 or 10.000000 MHz of 0.4 - 0.6 V into 300 Ohms to control instrument in con nection with item number 10.
10	This slide switch selects the internal or an external frequency standard. It must be set to "INT." if no external input is provided.
11	10 MHz standard frequency output of 0.4 V into 50 Ohms. This output may be used to "slave" other synthesizers not having internal standards.
12	Optional 1 MHz external frequency standard input, 0.4 V rms into 50 Ohms, used in connection with items 9, 10 and 13.
13	5 MHz frequency standard generated from external 1 MHz frequency standard applied at 12. The 5 MHz signal is connected to 9.
14	115/230 V ac line voltage selector switch.
15	Program connector for remote control of frequency and amplitude.

TABLE 2-1
CONTROLS AND INDICATORS

2-5. TYPICAL OPERATING PROCEDURES

a. Frequency Standard

The instrument may be operated from the internal standard, if so equipped; refer to the serial number tag on the rear panel, which indicates whether Option -01 or Option -02 internal standard is installed. If neither Option is installed, the instrument will not operate, unless an external standard signal is supplied to one of the rear - panel reference frequency input connectors.

CAUTION
If either Option -01 or Option -02 is installed, the standard frequency selection switch number 10, Fig. 2-1, must be set to INT.; otherwise no output will be obtained.

CAUTION
If neither Option -01 nor Option -02 is installed, the standard frequency selection switch number 10, Fig. 2-1, must be set to EXT. and an external 5.0 or 10.0 MHz signal must be supplied to the 5/10 MHz IN connector number 9, Fig. 2-1; otherwise no output will be obtained. If the optional 1 MHz external reference connector is installed, number 12, Fig. 2-1, then a 1 MHz reference may be used: apply 1 MHz to the connector and then connect the 5 MHz OUT, number 13, Fig. 2-1, to the 5/10 MHz IN, connector.

b. Warm-up & Frequency Stability

The instrument is operative on turn-on, as long as an internal or external standard is supplied, in accordance with the previous paragraph.

CAUTION
If the instrument is equipped with the Option -01 internal standard, a period of sixty (60) minutes is required at 25°C ambient for the output frequency to be within $\pm$ 1 x 10^{-7} of the frequency setting after ac power is connected. In the Standby mode, no warm-up is required.

c. Local Frequency Selection

The desired frequency is selected with the MHz, KHz and Hz selector switches. The highest output frequency obtainable is 159.9999999 MHz and the lowest recommended setting is 0.1000000 MHz. A frequency counter may be connected to the output connector to verify that the correct frequency is obtained.

CAUTION
For complete correspondence of dial settings and counter readings, the counter and the Model 5130A must be synchronized, i.e., slaved to the same frequency standard. This is accomplished by running the 5130 from the frequency standard of the counter, or vice versa. (See paragraph a. above).

d. Local Level Control

The Level control is used to set the desired level between +3 dBm (min) and +13 dBm (max) into 50 Ohms. An RF Voltmeter with a 50 Ohm load may be connected to the Output connector to set the level to the exact value desired.

2-6. REMOTE BCD FREQUENCY PROGRAMMING

a. Introduction

A 50-pin and 14-pin rear panel connectors are used to remotely control the frequency using BCD programming. The pin-out of each connector is given in Tables 2-2 and 2-3.

The 50-pin connector is used to control digits 0.1 Hz and higher, while the 14-pin connector is used for the 0.01 and 0.001 Hz digits. Phase continuity is not maintained when switching the 10 MHz, 1 MHz and 100 KHz digits. The output frequency is phase continuous when switching resolution digits 10KHz and lower.

The following paragraphs describe the differences and capabilities of switching non-phase and phase continuous digits. Also included is the description of an interface to a microcomputer data bus to demonstrate the simplicity and versatility of the remote BCD interface.

REMOTE BCD FREQUENCY CONTROL

Digit	BCD Weight 1	2	4	8	Latch Strobe (Hold Low For Storage)
10 MHz	15	16	40	41	23
1 MHz	17	18	19	20	24
100 KHz	1	2	26	27	24
10 KHz	3	4	28	29	25
1 KHz	5	6	30	31	25
100 Hz	7	8	32	33	46
10 Hz	9	10	34	35	46
1 Hz	11	12	36	37	47
0.1 Hz	13	14	38	39	47

Remote Enable: 42
Remote Enable GND: 49, 50
All functions above are negative true TTL.
DB Strobe: 43

REMOTE LEVEL CONTROL

Remote Level: 22; .6 V to 2.0 Volts for +3 to +13 dBm
Remote Level GND: 21

CAUTION

When front panel amplitude control is desired, the remote level line should be left open.

Table 2-2
REMOTE INTERFACE PIN ASSIGNMENTS
50 Pin Connector: Ansley 609-50F
(Mating Connector Supplied: Cinch 57-30500)

REMOTE BCD FREQUENCY CONTROL					
Digit	BCD Weight				Latch Strobe
	1	2	4	8	
.01 Hz	8	9	7	6	Use DB Strobe
.001 Hz	10	11	5	4	Pin 43 (See Table 2-2)
Remote Ground 13					

Table 2-3
REMOTE INTERFACE PIN ASSIGNMENTS
14 Pin Connector: Ansley 609-14F
Mating Connector Supplied: Amphenol 57-30140

b. Remote Programming Non-Phase Continuous Digits

The Model 5130A output frequency does not switch phase continuously when switching the 10 MHz, 1 MHz, and the 100 KHz frequency digits. When these digits are to be switched, no strobe pulse is necessary. Simply changing the BCD data will cause the output frequency to change.

"7475 TTL" latches are provided for these digits with an individual strobe connected to the 1 MHz and 100 KHz digit. The strobes have "pull up" resistors. If the strobes are not connected, data will pass through the latch. If the strobe lines are brought low (ground), the digits frequency information is stored and any further activity on the data lines for that digit will not alter the output frequency.

c. Remote Programming Phase Continuous Digits

A data strobe pulse (DB Strobe) is required to enter data into the frequency register for all digits from the 0.001 Hz decade to the 10 KHz decade. These are the frequency digits that can be remotely switched phase continuously.

Set the remote BCD data lines to the desired frequency and strobe the DB Strobe line, pin 43,on the remote connector. The output frequency will switch phase continuously from the old to the new frequency after a short delay (3 μsec nominal). The delay can be measured from the rising edge of the DB Strobe pulse.

d. Remote Programming All Digits Simultaneously

When it is desired to have the frequency of all digits (.001 Hz through 10 MHz) change simultaneously connect a 1 μsec positive going TTL pulse to the 10 MHz strobe, 1 MHz and 100 KHz strobe, and DB Strobe lines together (pins 23, 24 and 43). This will synchronize data changes for all the digits.

e. Interfacing to a Microcomputer Data Bus
(See Block Diagram and Timing Diagrams, Figs. 2-2 & 2-3)

Data can be entered from a microcomputer data bus in a byte serial fashion and still have the 0.001 Hz through the 10 KHz digits switch the output frequency phase continuously because of the use of double buffers. The double buffered decades, 0.1 Hz decade through 10 KHz decade, have "7475 TTL" latches with a strobe for every two decades. The latches are called the input buffer. Each strobe has a "pull-up" resistor so that if they are not connected data will pass through the latches to a second register, called the frequency register. The frequency register uses one strobe line "DB Strobe" to enter data for the 0.001 Hz digit through the 10 KHz digit. Note that the 0.001 Hz and 0.01 Hz digits need not be double buffered. They can be strobed last in the byte serial sequence with the DB Strobe.

To enter data in a byte serial fashion, connect the "1" bit weights of the 0.001 Hz digit through the 10 KHz digit together, then connect the "2" bit weights together, etc. Use the individual digit strobes to enter the data in their proper latches. After all the data latches are loaded use the DB Strobe to enter the data into the frequency register. The output frequency will now change phase continuously using all the data that is stored in the input buffer.

2-7. REMOTE LEVEL PROGRAMMING

To remotely program the output level, the following procedures should be performed:

1. Rotate the front panel level control full counter clock-wise, so that the switch "clicks".

2. Apply a DC voltage to Pin 22 of the rear panel connector. (Pin 21 is the ground return).

3. The output level will vary from +3 to +13 dBm for a corresponding input of +0.6 to +2.0 Volts.

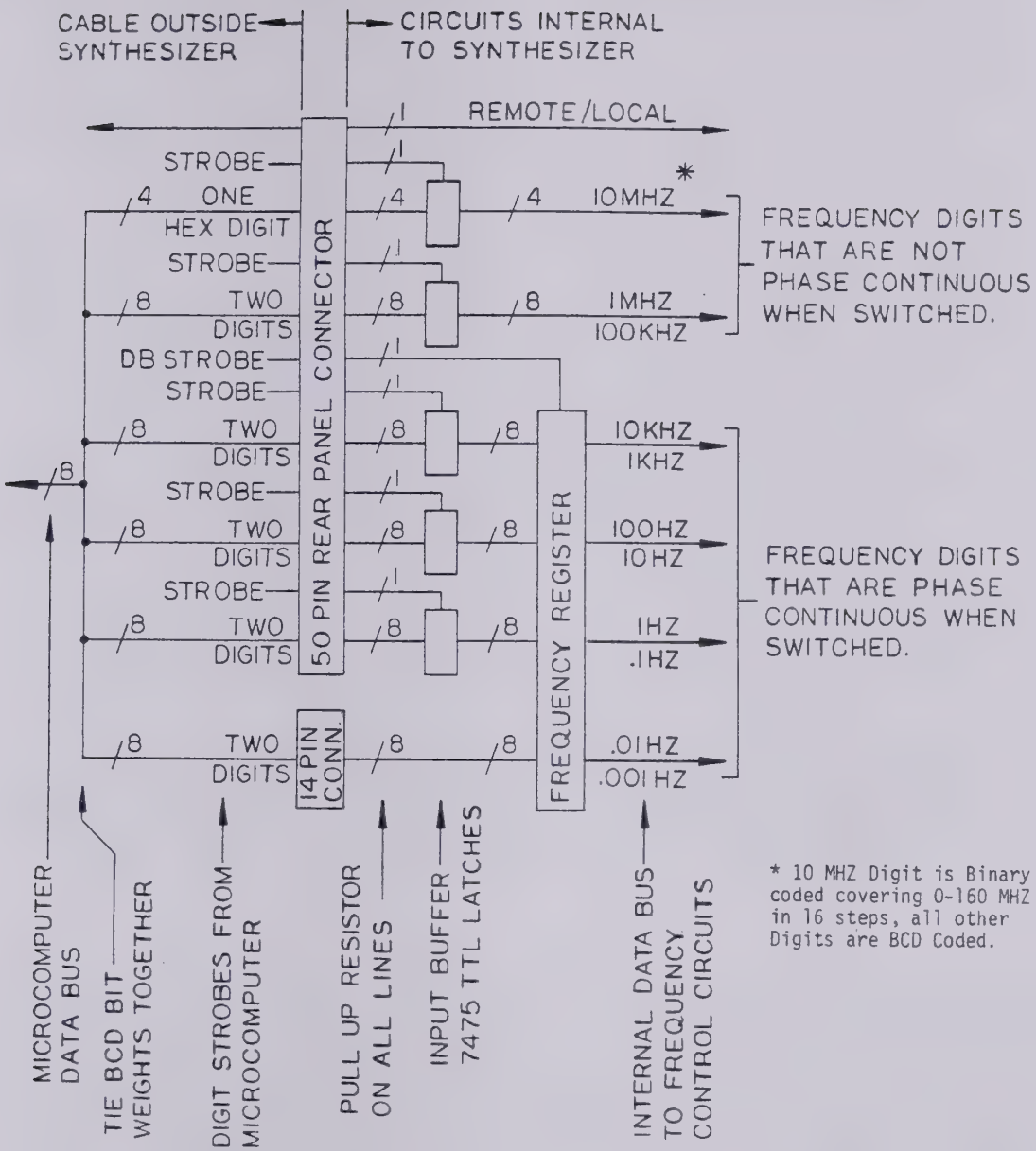


Fig. 2-2 Block Diagram Showing Interface
To Microcomputer Data Bus

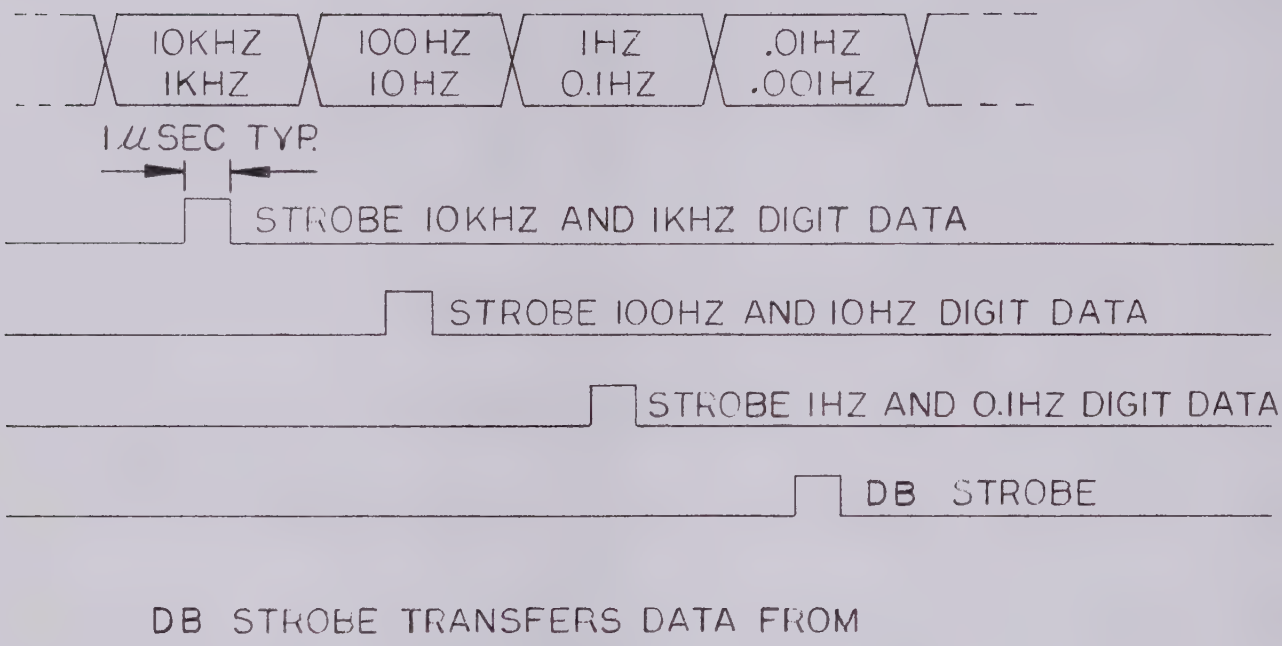


Fig. 2-3 Timing Diagram For Interface To Microcomputer Data Bus

SECTION 3

PRINCIPLES OF OPERATION

3-1. GENERAL

This section provides an overview of operating principles by discussing the block diagram in Fig. 3-1. Detailed module descriptions are found in subsequent sections. The material presented here is essential for efficient service and familiarity with it is assumed in the service instructions.

All output frequencies of the 5130A are derived from the crystal oscillator by arithmetic operations and are fully coherent with the standard 10 MHz frequency. The instrument uses a simplified direct synthesis in which all auxiliary fixed frequencies are produced from a 10 MHz pulse. The final output frequency comes for a beat-frequency system: a signal of 365 - 355 MHz, which carries all 0.001 Hz to 1 MHz steps, is subtracted from a 365 to 515 MHz signal which carries the 10 MHz steps. The resultant output ranges from 0.1 MHz to 160 MHz. The 0.1 MHz is the practical cutoff in the output amplifier, lower frequencies could otherwise be obtained. Strictly speaking, 160 MHz is not a settable output, but for simplicity in discussing bandwidths, the 0.001 Hz difference is neglected.

The block diagram shows a crystal oscillator which is the prime reference in the system and three sections: a standard frequency section, a fine resolution section and a 10 MHz step section; an output amplifier completes the system.

3-2. STANDARD FREQUENCY SECTION

This section consists of the Standard Generator A (SGA) and Standard Generator B (SGB) modules; they provide all fixed standard frequencies needed and operate from an input of 10.000 MHz, (or 5 MHz which is automatically doubled). For either input a filtered 10 MHz signal is fed to a pulse generator, where harmonics of 10 MHz up to 140 MHz are generated with equal amplitude. This "picket fence" is the basis for all fixed standard frequencies. The SGA and SGB modules supply: 14, 16, 18, 20, 22, 112 and 113 MHz for use in the fine resolution section. The 10 MHz picket fence from the SGA module is also fed to the 10 MHz - step section. The above frequencies all stem from arithmetic operations on the original 10 MHz multiples.

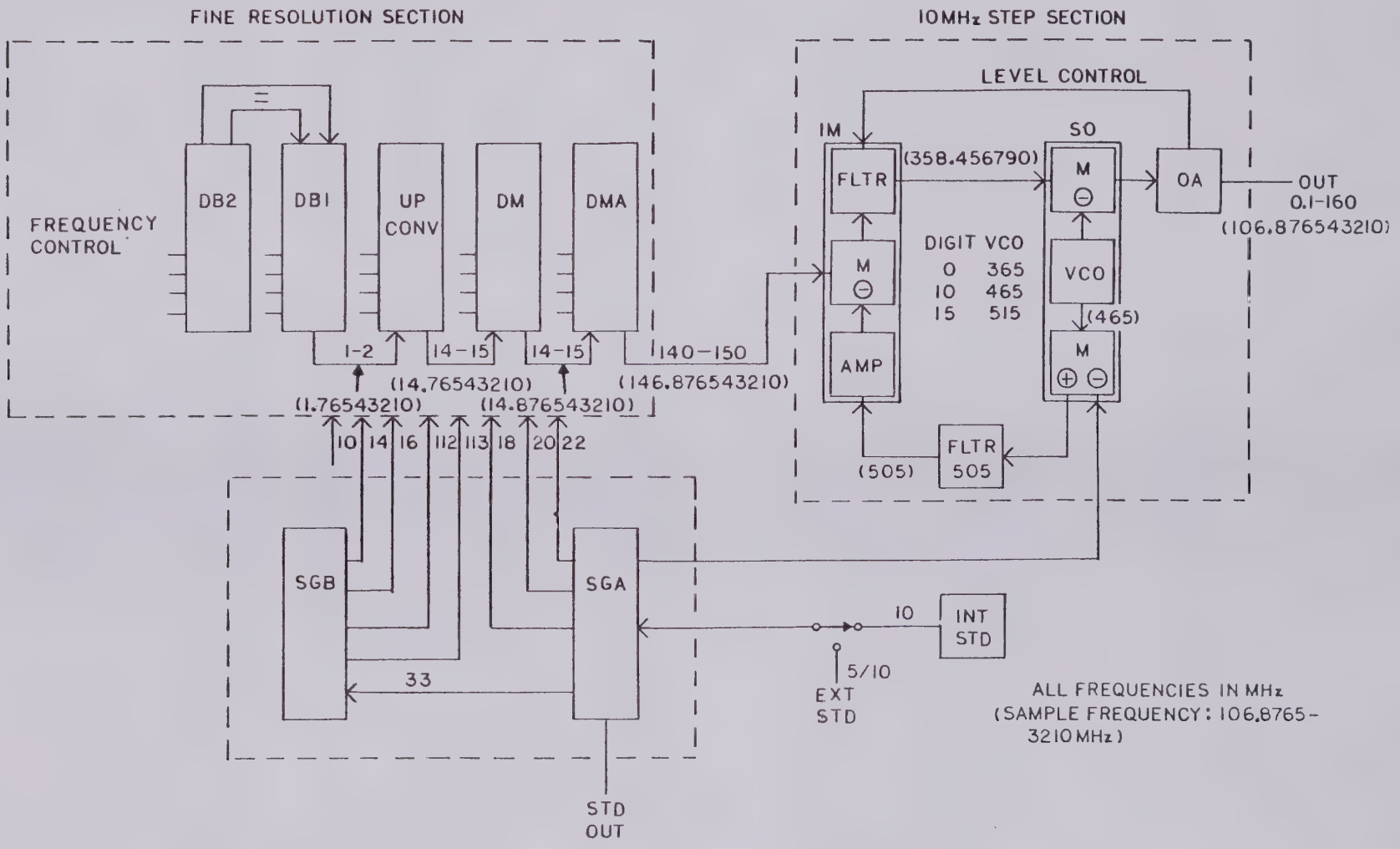


FIG 3-1 MODEL 5130A BLOCK DIAGRAM

3-3. FINE RESOLUTION SECTION

Frequencies, 1 MHz and below, are produced in this section. The lowest decades, 0.001 Hz through 10 KHz are generated by the DB 1 and 2 modules. DM adds the 100 KHz decade, while the DMA adds the 1 MHz decade. These modules are connected in series so that as the signal progresses, starting from the DB through the DMA, the decade steps are added.

DB 1 and 2 produce a carrier between 1 and 2 MHz where the decades below 1 MHz correspond to the decades 0.001 Hz to 10 KHz at the final output. For example, if the final output selected is 0.876543210 MHz, then the output of DB 1 will be 1.76543210 Hz. The Upconverter then translates this signal to 14.76543210 MHz. The next decade, 100 KHz, is added in the DM module so its output is 14.876543210 MHz which feeds the DMA. The DMA module adds the 1 MHz steps and also transfers the information to a frequency which can carry a 10 MHz bandwidth more readily. The "carrier" at the output of the DMA is 140 MHz and if the above selected frequency is expanded to say 6.876543210 MHz, then the output of the DMA is 146.876543210 MHz.

3-4. 10 MHZ STEP SECTION

In this section frequencies are used which are not standard-frequency derived. Frequencies mentioned in the previous paragraphs were all as accurate as the standard 10 MHz frequency. In this section the Voltage-Controlled Oscillator (VCO) frequencies from 365 to 515 MHz (in 10 MHz steps) may differ from their nominal values by as much as 1 MHz; as will be shown, such deviation from the absolute value has no effect on the output frequency. The "Stepped Oscillator" (SO) operates in a drift-cancelled loop which serves two functions:

1. Selection and filtering of one of fourteen 10 MHz pickets by a fixed 505 MHz filter.

2. Supply of frequencies high enough for the final mixer, with a high degree of coherence in the two mixer inputs.

The block diagram shows some of the VCO frequencies corresponding to certain 10 MHz steps as examples. These will be helpful in recognizing the complete synthesis process via a sample frequency.

If we return to our previously chosen sample frequency in the fine resolution section of 146.876543210 MHz and assume that we have set the 10 MHz dial to 10, our complete frequency setting is 106.876543210 MHz. As shown in the block diagram for the "10" step the VCO will produce a frequency of 465 MHz, which is fed to two different mixers. In the mixer near the 505 MHz filter the "picket fence" line of 40 MHz will add to the 465 MHz and feed 505 MHz through the filter and into the Intermediate Mixer(IM). After this mixer the lower side-band of 505 and 146.876543210 is filtered out by a 355 - 365 MHz band-pass filter; in this case the frequency is 358.123456790 MHz. This frequency enters the output mixer, where it is subtracted from the VCO frequency

of 465 MHz. The resultant difference is 106.876543210, our selected output frequency. After a low-pass filter the output frequency is amplified in the Output Amplifier (OA) and fed to the output connector.

As can be seen, the VCO feeds both inputs to the final mixer, one directly, one after an intermediate mix. Therefore, if the VCO frequency deviates from nominal, both mixer inputs move up or down in frequency together by the same frequency increment. This obviously does not alter the difference of these two frequencies, which is the desired output frequency.

SECTION 4

MAINTENANCE, SYSTEM LEVEL

4-1. INTRODUCTION

No preventive maintenance is required for the 5130A Frequency Synthesizer. For convenience of service all modules are easily removed from the deck and replaced. It is the purpose of this section to provide information which in case of malfunction permits the identification of a defective module.

The preferred service procedure is the exchange and factory-service of the module.

4-2. RECOMMENDED TEST EQUIPMENT

Test equipment recommended for troubleshooting is listed below:

RF Voltmeter "V" "V50"	1-600 MHz, 10 mV - 1 V, High Impedance Probe (3 pF, D.C. Res. 100 K Ohms) 50 Ohm terminated "T" Coax Adapter
HF Counter "C"	0 - 200 MHz or 0 - 20 MHz, 10 mV Sensitivity, High Impedance or 50 Ohm Input, 10 Hz Resolution Input for External Drive for Synchronization with 10 MHz, 0.5 V into 50 Ohms or more
Spectrum Analyzer "SA"	0 - 505 MHz, 50 Ohm IMPEDANCE, 70 dB on-screen dynamic range. Resolution 1 KHz minimum. Sensitivity -40 dBm FS in 10 dB LOG display.
Multimeter	Analog or Digital, 0 - 15 V, 0.1 V Resolution, 0 - 2 A, 0.1 A Resolution.

Note:

Test equipment is referenced in Table 4-1 as noted above (V", "C", "SA"). The Voltmeter and Counter must have high DC input resistance since connection is made to points with +5.4 V potential. The RF-Voltmeter probe connects directly to test points. The Counter is connected via a RG-174 or similar small RF cable equipped with small alligator clips.

4-3. TROUBLESHOOTING PROCEDURES

If there is no output from the instrument, proceed as follows:

With instrument connected to the power line, power switch in the "ON" position, either the "Remote" or "Local" indicator light should be on. Check fuse if no indication is obtained. Use only fuse of proper rating to replace. If indicator light is on, set instrument to the "Local" mode, and dial desired frequency; if no output is obtained, check rear panel output "Standard Frequency", 10 MHz output where 0.4 - 0.5 V into 50 Ohms should be obtained. If no output is present (and the instrument is equipped with an internal standard and set to "INT". STD.") the bottom cover of the instrument has to be removed.

WARNING
DISCONNECT UNIT FROM POWER LINE. (STANDBY POWER IS PRESENT WITH POWER SWITCH OFF.)

Remove two screws holding the lip on the rear panel and carefully withdraw cover. To fully withdraw from case, cover has to be deflected in the middle, so that fold-down stand screws clear rear panel.

After unit is powered again, check for presence of supply voltages -12.4 V (Yel. wire) and +5.4 V (Red wire) at the terminals of the power supply on the rear panel. If voltages are within ±0.2 V, proceed; if voltage is absent or low, measure current in the leads from the supply. The proper 5.4 V current is 2A nominal. -12.4 Volt power is distributed to two places from the power supply. One branch is used for the standby mode which powers the crystal oven. The current is nominally 0.2A depending on crystal oven temperature. The other branch is routed through the front panel power switch and supplies power, 0.8A nominal, to the synthesizer. In standby, -12.4 Volts is not supplied to the synthesizer. It is routed back to the power supply to disable the +5.4 output.

If the output is still absent or incorrect, the measurements shown on Table 4-1 are made; Table 4-1 lists test points, signal frequencies and levels. Fig. 4-1 shows location of test points and Fig. 4-2 is a top view of the instrument showing the location of all modules and mainframe assemblies.

To run a full diagnostic check, all the instruments with the upper frequency limits are required. It is possible, however, to test most of the instrument with the RF-Voltmeter and the 20 MHz Counter.

Proceeding from the crystal oscillator through the Standard Frequency Section and the Fine Resolution Section most tests for presence of a signal and proper frequency can be made by "bridging" (without opening connections). These checks cover the bulk of the instrument. To check signals in the 10 MHz step section and the output amplifier 50 Ohm SMA connections have to be made.

Test Point	Frequency (MHz)	Nominal Level	Test Equipment	Module Checked	Notes
SGA, 51	10.000	0.4 V	V,C	SO	
SGA, 49	10.000	0.4 V	V,C	SGA	
SGA, 20	18.000	0.1 V	V,C	SGA	
SGA, 43	20.000	0.1 V	V,C	SGA	
SGA, 6	22.000	0.1 V	V,C	SGA	
SGA, 2	33.000	70 mV	V,C	SGA	3
SO, J1	10-140	-17 dBm	SA	SGA	
SGB, 10	14.000	0.1 V	V,C	SGB	
SGB, 24	16.000	0.1 V	V,C	SGB	
DMA, 1	112.000	0.15 V	V,C	SGB	
DMA, 10	113.000	0.15 V	V,C	SGB	
DM, 50	14.000	0.25 V	V,C	DM	2
DMA, 50	140.000	0.40 V	V,C	DMA	2
Filter Output	505±1 MHz	-35 dBm	SA	SO, Filter	
IM, J38	355±1 MHz	-16 dBm	V,SA	IM	
SO, J39	100.000	-25 dBm	SA	SO	2
OA, J32	100.000	+13 dBm	S,V50	OA	2
UC, J15	1 MHz	-16 dBm	V,C	DB1,2	2
UC3	14.000	0.25 V	V,C	UC	2

Notes:

1. Test point designations show the module type and the pin number (position) of the board-edge connector, as used on the module schematic.
2. Set instrument to 100.000000 MHz.
3. Disconnect SMA connector and connect SA in place of SO at J1. Each 10 MHz multiple from 10 to 140 MHz to be displayed.

TABLE 4-1 TROUBLESHOOTING CHART

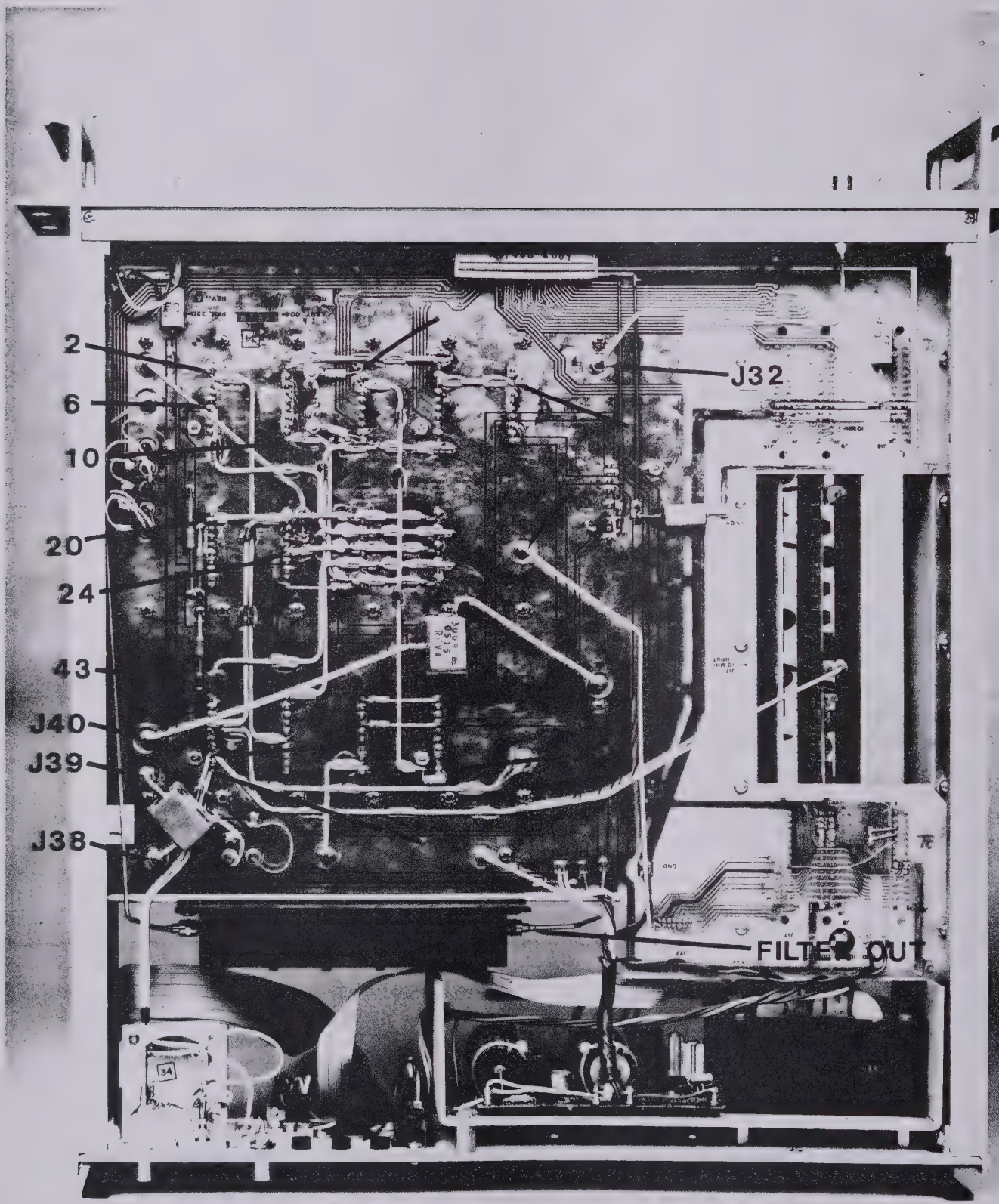


Fig. 4-1 Location of Test Points

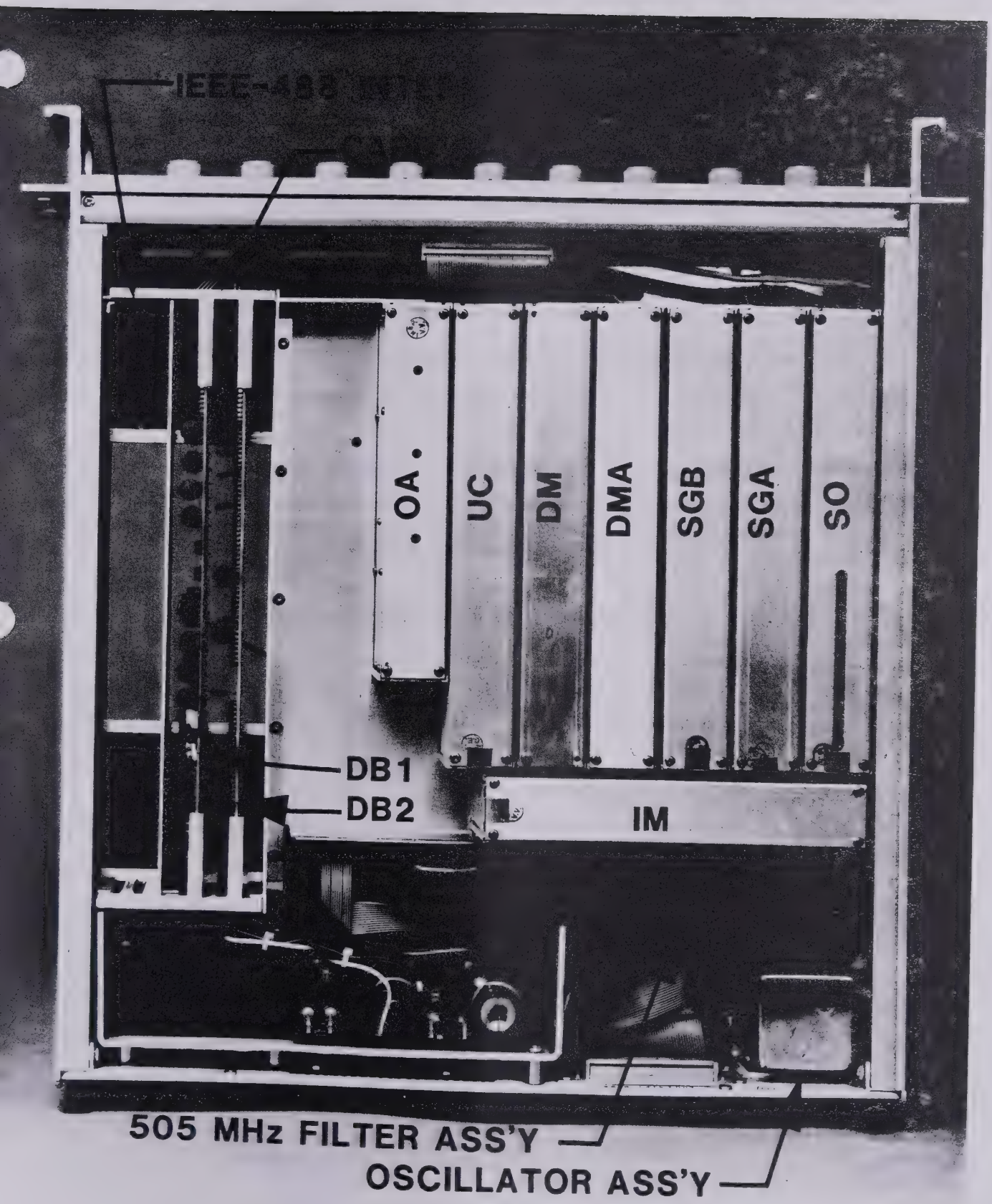


Fig. 4-2 Modules and Mainframe Assemblies

4-4. MAINFRAME ASSEMBLIES

4-4-1. Power Supply Assembly, P/N 174.5007

The Power Supply Assembly generates DC voltages of +5.4 V and -12.4 V. The former is used for TTL and MECL logic (fed by decoupling networks), and the -12.4 V powers the transistor amplifiers.

The two regulators are fed from one transformer with a split primary; they are similar, and both have capacitor input filters fed by silicon rectifiers. The regulators which follow consist of a series-pass power transistor and integrated circuits which contain the reference and gain elements. Both supplies are short-circuit proof and have fold-back current limiting.

In case of malfunction the schematic which lists essential DC voltages may be used to locate the faulty component or replace the power supply assembly as a unit. Component reference designations are screened on the power supply printed circuit board.

4-4-2. Crystal Oscillator Assembly

The Wavetek Rockland Model 5130A may be supplied with a built-in oven-type or TCXO crystal oscillator operating at 10 MHz. It is mounted on the instrument rear panel and has the following characteristics:

	P/N 173.6003 Proportional Oven Control	P/N 173.6002 Moderate Stability TCXO
Frequency:	10.000000 MHz	10.000000 MHz
Aging:	$\pm 2 \times 10^{-9}$ / day	$\pm 1 \times 10^{-8}$ / day
Output:	1 V rms into 500 Ohms	0.5 V into 50 Ohms
Temperature Stability:	$\pm 1 \times 10^{-8}$, 0°C to 50°C	$\pm 1 \times 10^{-6}$, 0°C to 50°C
Warm-up Time:	24 hours for 1×10^{-8}	
DC Supply:	-12.4V, 250 mA (500 mA turn-on)	-12.4 V, 20 mA

In case of malfunction, the Crystal Oscillator Assembly must be replaced.

4-4-3. Front Panel Board Assembly, P/N 004.5602

The Front Panel Board Assembly is mounted to the front panel and is directly connected with the Amphenol 57 type program input connector through a 50 conductor ribbon cable. It contains frequency select switches and circuitry to interface the outside programming signals for frequency control with the modules in the instrument. It also effects the transfer from local to remote frequency control with the Remote Enable command. The remote programming format is parallel entry, 1, 2, 4, 8 BCD for each digit. TTL logic levels are used and all commands are negative true. The 7475 type latches provide storage when this mode of operation is desired. To store a program input, the Storage Enable pins must be brought to the low state. Table 2-2 indicates pin assignments in the last column. Note that four enable lines are provided so

that serial operation of the 4- or 8- bit bytes is possible. With reference to the Schematic Diagram, U10 is used to control a switch consisting of three transistors. U10 accepts the Remote Enable signal which is normally negative true. U1 to U9 perform the digit storage and are only powered when the instrument is in the remote mode; otherwise 5.0 V is supplied to the front-panel switches only. Pin assignment in the 57-40500 connector is shown in Table 2-2.

4-4-4. Remote Front Panel Board Assembly, P/N 004.5603

This assembly is mounted to the front panel in models without manual controls. Program format is compatible with the standard front panel board assembly, including the use of Table 2-2. The exceptions are the elimination of manual controls and digital control of the Remote Enable command, which is not used.

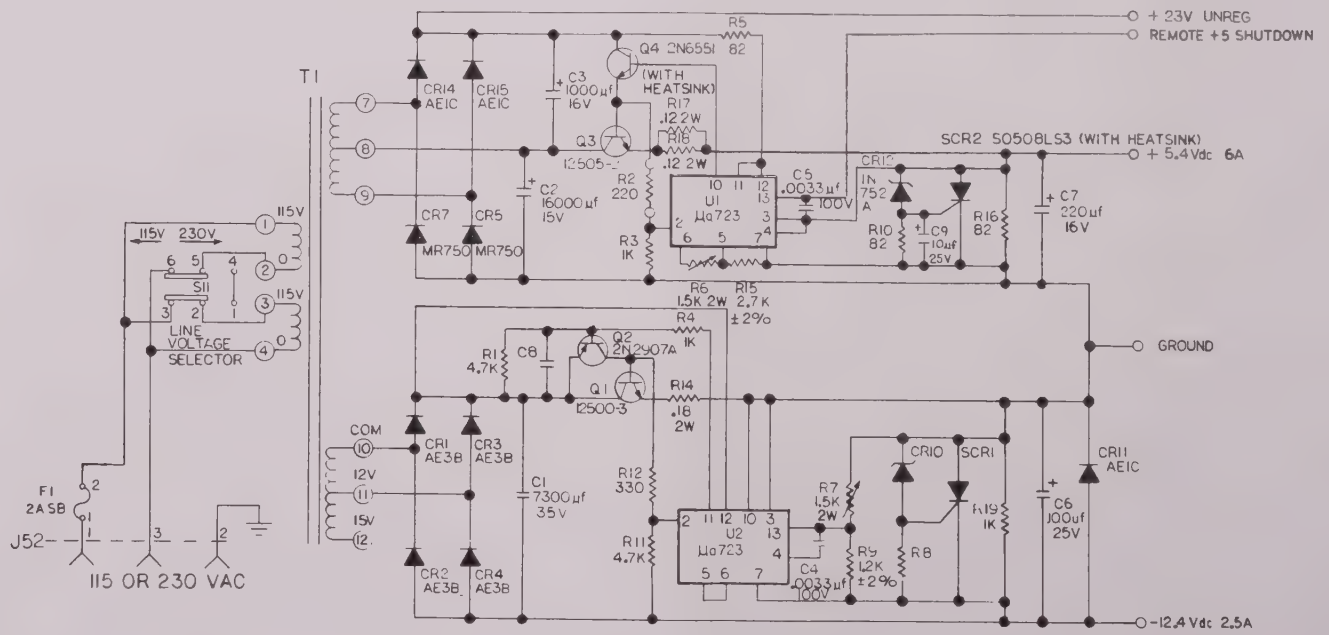
4-4-5. 505 MHz Filter Assembly, P/N 165.3006

This 5 - section cavity filter forms part of the 10 MHz step section. It is fixed-tuned and cannot be retuned in the field. It is bolted to the back lip of the deck.

In case of malfunction, the Filter Assembly must be replaced.

4-4-6. Mainboard Assembly

The Mainboard Assembly is used to distribute power and signals from module to module. These connections are made with printed circuit runs or semirigid coaxial cable. The modules plug into printed circuit connectors that are soldered to the mainboard assembly and each module is held in place with three screws that provide good mechanical stability and electrical grounding. The mainboard assembly drawing and schematic can be used to identify and trace signals that interconnect modules.



NOTES

1. UNLESS OTHERWISE SPECIFIED, ALL RESISTORS ARE IN OHMS, $\frac{1}{2}$W, ±5%.

(2. MFG P/N HCC512)

SIZE	DWG NO	REV
C		

LTR	ECO NO	CHANGED BY	APPV'D BY	DATE
A	RELEASE			11/29/91
B	1220	7-8-91	LAT	7/29/91

DRAWN BY		DATE 7/5/90
CHECKED BY		
ENG APPVL		11/27/91
MFG APPVL		11/27/91

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AFTER FINISHING AND TOLERANCES ARE:
.XXX ±
.XX ±
X/n ± 1/64
∠° ± 1°

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TITLE
SCHEMATIC
POWER SUPPLY

SIZE	DRAWING NO.	REV
C	03 174 5007	B

SCALE — SHEET 1 OF 3

REPLACEABLE PARTS LIST

PC BD ASSY, FRONT PANEL
P/N 004.5602

Ref. Des.		Description	P/N
CR1 thru CR36	CR:	S1 cmptr 75 PIV (1N4151)	132.4151
DS1, DS2	LED:	Green	171.1602
J57, J58	Conn:	Term 50 pin Dil St	354.0021
Q1	Q:	Sil PNP (2N2905)	136.2905
Q2, Q3	Q:	Sil PNP (2N3250)	136.3250
R1,R2,R5,R8	R:	Fxd cflm 2.2 K Ohm 5% 1/4W	116.2221
R3	R:	Fxd cflm 220 Ohm 5% 1/4W	116.1221
R4	R:	Fxd cflm 470 Ohm 5% 1/4W	116.1471
R6	R:	Fxd cflm 150 Ohm 5% 1/4W	116.1151
R7	R:	Fxd cflm 10 K Ohm 5% 1/4W	116.3101
R9	R:	Fxd mflm 1.99 K Ohm 1% 1/10W	111.1990
R10	R:	Fxd mflm 100 K Ohm 1% 1/10W	113.1001
R11	R:	Fxd mflm 340 Ohm 1% 1/10W	110.3401
S2,S3,S4,S5 S6,S7,S8,S9	S:	Rot 10P BCD 36 deg P.C. mt	345.1103
U1 thru U9	U:	4 Bit Latch (7475)	122.7475
U10	U:	Hex Inverter (7404)	122.7404
U11,U12	U:	Pull-up Net 661-1-2.2K 2% x 15	128.2221
U13,U14,U15	U:	Pull-up Net 661-1-10K 2% x 15	128.3101

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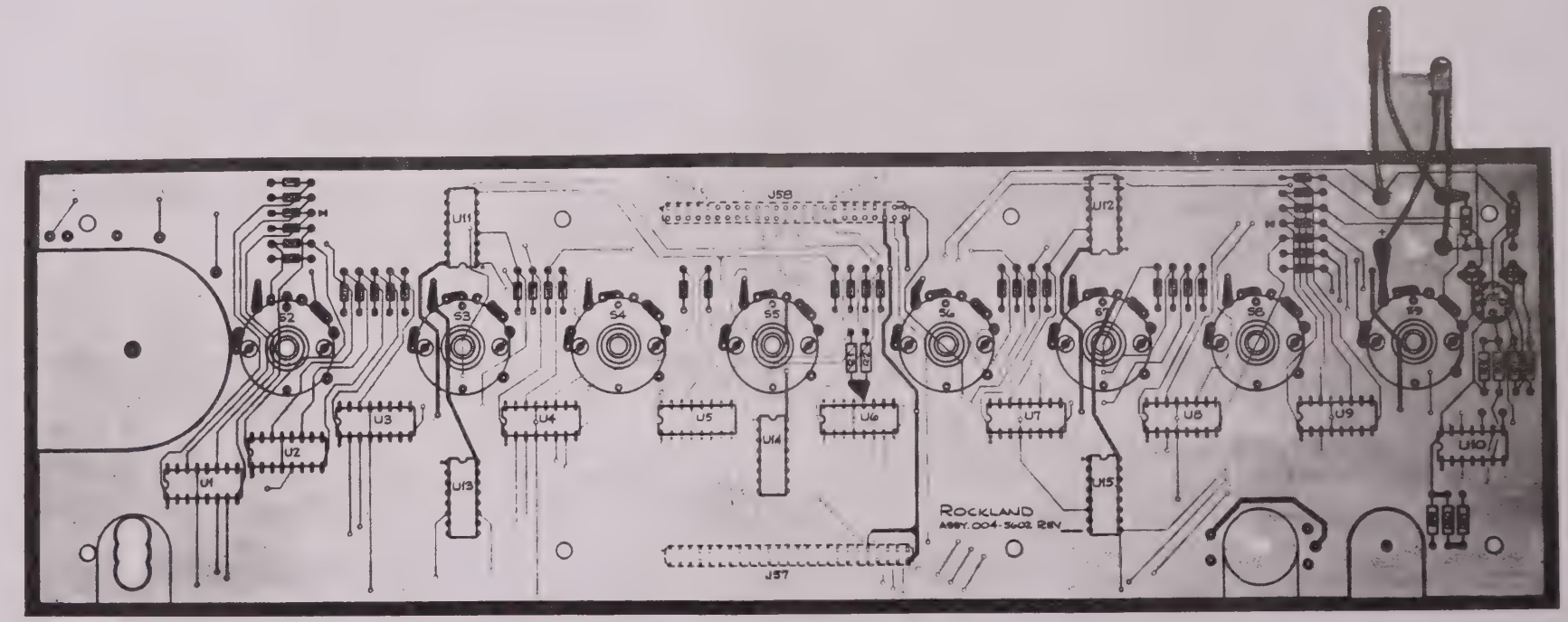
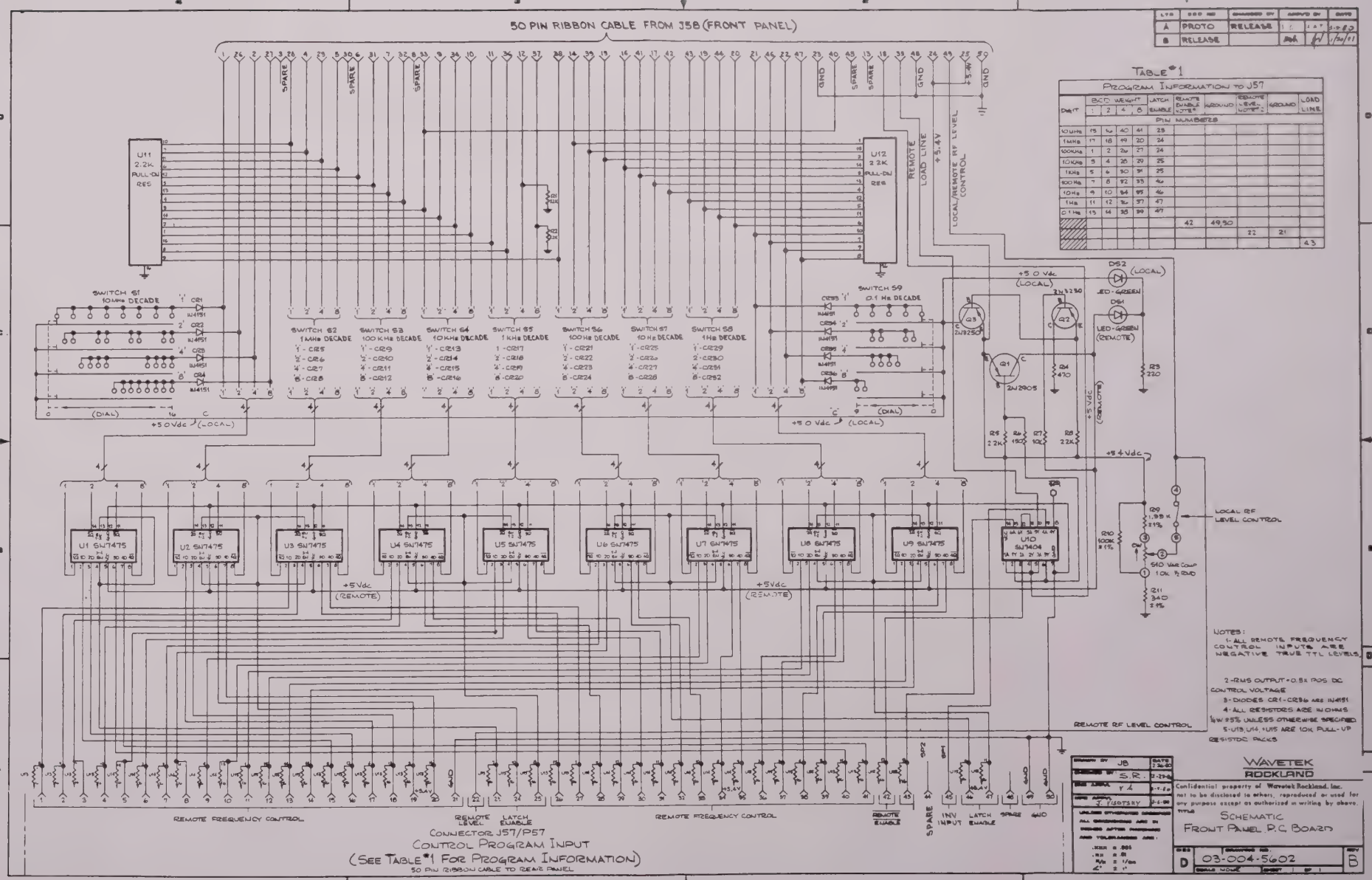
ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK ROCKLAND	Wavetek Rockland, Inc.
MATERIAL	DRAWN	TITLE	ASSEMBLY FRONT PANEL P.C.B.
FINISH	CHKD		
	ENG APPR		
	MFG APPR	SIZE D	MODEL NO. 5130/2102 DRAWING NO. 02-004-5602 REV C
	ISSUED	SCALE	CODE IDENT 23338 SHEET OF


50 PIN RIBBON CABLE FROM J58 (FRONT PANEL)
TABLE #1
PROGRAM INFORMATION TO J57
U11 2.2K PULL-DN RES
U12 2.2K PULL-DN RES
SWITCH S1 10 MHz DECADE
SWITCH S2 1 MHz DECADE
SWITCH S3 100 KHz DECADE
SWITCH S4 10 KHz DECADE
SWITCH S5 1 KHz DECADE
SWITCH S6 100 Hz DECADE
SWITCH S7 10 Hz DECADE
SWITCH S8 1 Hz DECADE
SWITCH S9 0.1 Hz DECADE
+5.0 Vdc (LOCAL)
+5 Vdc (REMOTE)
+5.4 Vdc
U1 SN7475
U2 SN7475
U3 SN7475
U4 SN7475
U5 SN7475
U6 SN7475
U7 SN7475
U8 SN7475
U9 SN7475
U10 SN7404
LOCAL RF LEVEL CONTROL
REMOTE RF LEVEL CONTROL
REMOTE FREQUENCY CONTROL
REMOTE LATCH ENABLE
SPARE
INV. INPUT
GND
CONNECTOR J57/P57
CONTROL PROGRAM INPUT
(SEE TABLE #1 FOR PROGRAM INFORMATION)
50 PIN RIBBON CABLE TO REAR PANEL
NOTES:
1. ALL REMOTE FREQUENCY CONTROL INPUTS ARE NEGATIVE TRUE TTL LEVELS.
2. RMS OUTPUT = 0.5 x POS DC CONTROL VOLTAGE
3. DIODES CR1-CR96 ARE IN4151
4. ALL RESISTORS ARE IN OHMS 1/8W ±5% UNLESS OTHERWISE SPECIFIED
5. U13, U14, U15 ARE 10K PULL-UP RESISTOR PACKS
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SCHEMATIC
FRONT PANEL P.C. BOARD
03-004-5602
B

REPLACEABLE PARTS LIST

PC BD ASSY, REMOTE PROGRAM
P/N 004.5603

Ref. Des.		Description	P/N
C1 thru C5	C:	Fxd mono 0.1 uF 50V Z5U	100.4102
J57, J58	Conn:	Term 50 Pin Dil St	354.0021
U1 thru U9	U:	4 Bit Latch (SN7475)	122.7475
U10 thru U15	U:	Pull-up Net 764-1-10 K 2% x 7 Sip	128.3105

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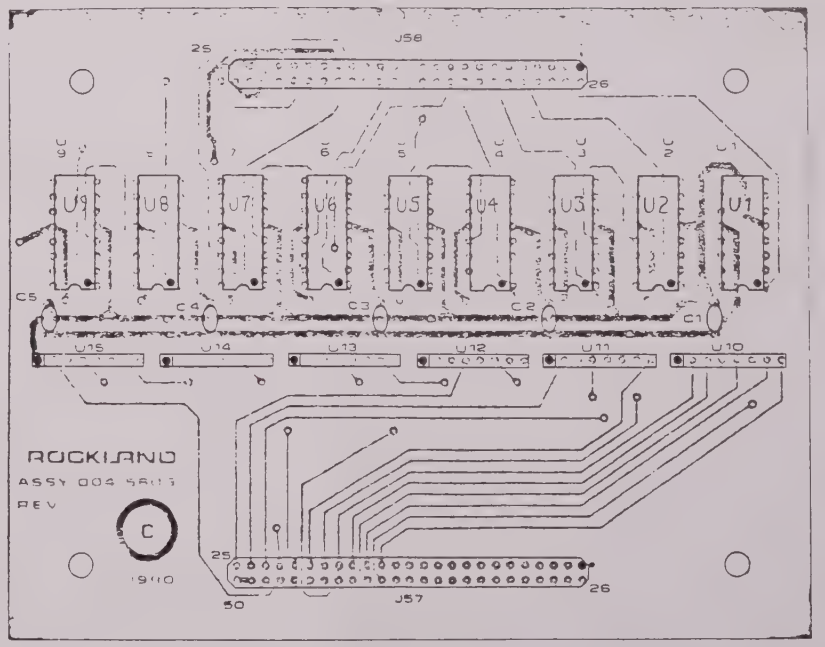
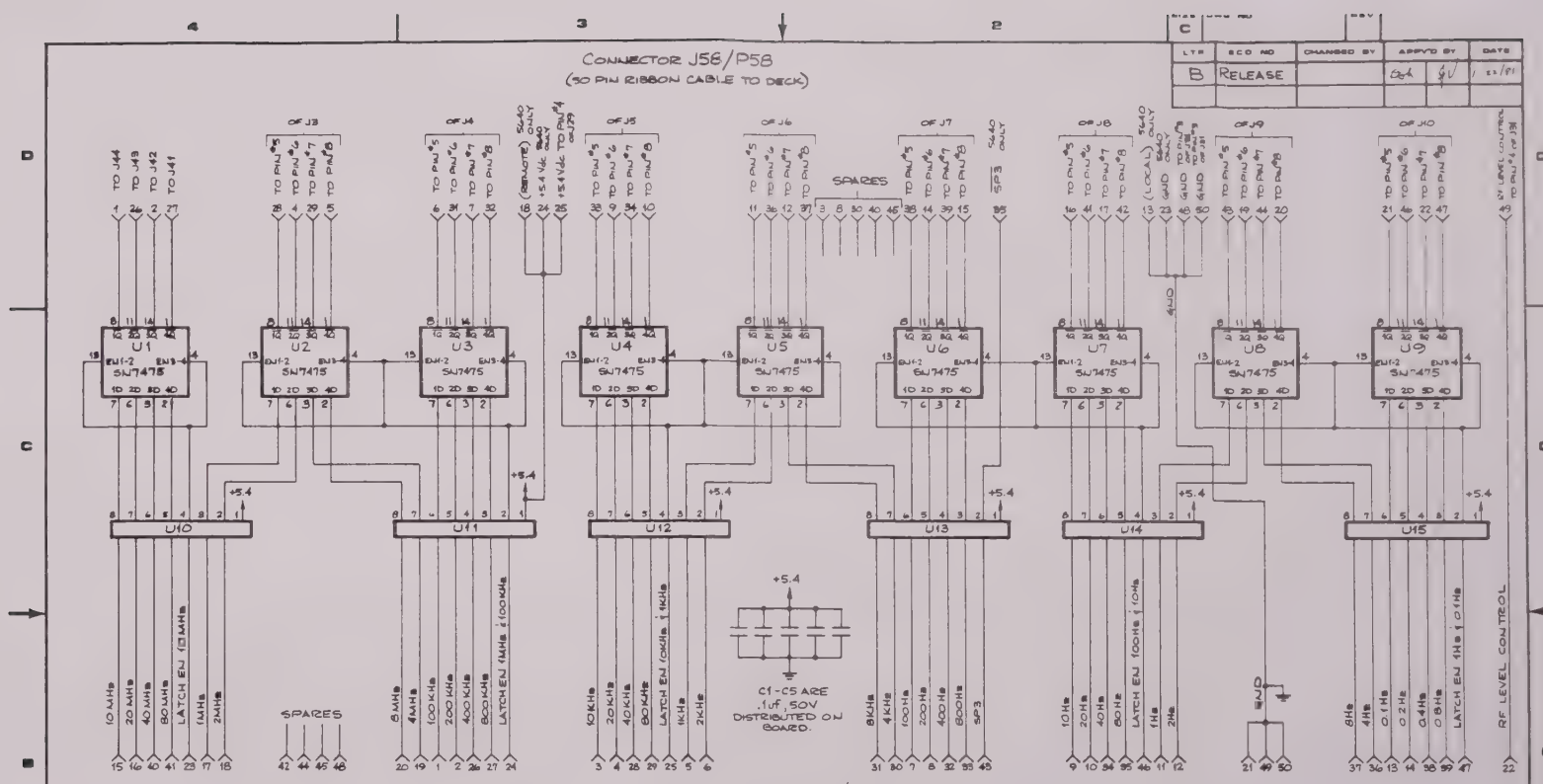
ZONE	LTR	ECO NO	CHANGED BY	APPR D BY	DATE



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE		DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK ROCKLAND Wavetek Rockland, Inc.
x/x ± 1/64 | xxx ± .005 | xx ± .01 | ∠ ± 1°		DRAWN / DATE	TITLE: PCB ASSY REMOTE PROGRAM
MATERIAL		CHKD	
		ENG APPR	
FINISH		MFG APPR.	SIZE: C | MODEL NO: 5130/20 | DRAWING NO: 02-004-5603 | REV: A
		ISSUED	SCALE | CODE IDENT: 23338 | SHEET OF

D C B A

4 3 2 1



CONNECTOR J57/P57
(50 PIN RIBBON CABLE TO REAR PANEL)
CONTROL PROGRAM INPUT
(SEE TABLE #1 FOR PROGRAM INFO.)

TABLE #1

PROGRAM INFORMATION TO J57

DIGIT	BCD WEIGHT 1	2	4	8	LATCH ENABLE	REMOTE ENABLE NOTE #1	GROUND	REMOTE LEVEL NOTE #2	GROUND
	PIN NUMBERS								
10 MHz	15	16	40	41	23				
1 MHz	17	18	19	20	24				
100 KHz	1	2	26	27	24				
10 KHz	3	4	28	29	25				
1 KHz	5	6	30	31	25				
100 Hz	7	8	32	33	46				
10 Hz	9	10	34	35	46				
1 Hz	11	12	36	37	47				
0.1 Hz	13	14	38	39	47				
						42	49,50		
								22	21

NOTES:
1 - ALL INPUT FUNCTIONS ARE NEGATIVE TRUE, TTL.
- ALL OUTPUT FUNCTIONS ARE POSITIVE TRUE, TTL.
LEVELS: LOW +0.7V MAX.
HIGH +2.0-5.0V
2 - RMS OUTPUT = 0.5 x POS. DC CONTROL VOLTAGE.
3 - U10-U15 ARE 8-PIN SIP RESISTOR PULL-UP NETWORKS, 7 x 10K OHMS, 2%.
4 - FOR IC SN7475, VCC = PIN #5, GND = PIN #12.

LTR	ECO NO	CHANGED BY	APPVD BY	DATE
B	RELEASE			1/23/81

DRAWN BY	JB	DATE 8-20-80
CHECKED BY		
ENG APPVL		11/23/81
MFG APPVL		11/23/81

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AFTER FINISHING AND TOLERANCES ARE
.XXX ±
.XX ±
X/X ± 1/64
∠° ± 1°

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TITLE
SCHEMATIC
REMOTE PROGRAM

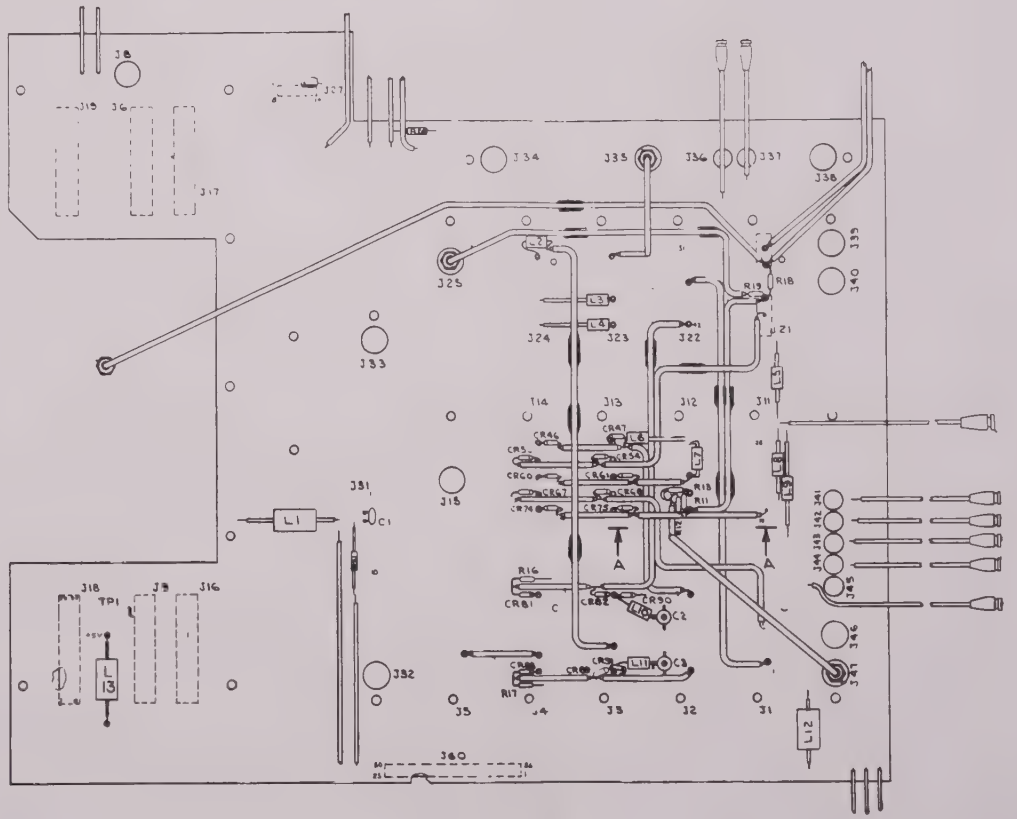
SIZE	DRAWING NO.	REV
C	03-004-5603	B
SCALE NONE	SHEET 1 OF 1	

REPLACEABLE PARTS LIST

PC ASSEMBLY MAINBOARD
P/N 004.5129

Ref. Des.		Description	P/N
C1	C:	Fxd cer .1 uF +80 -20% 12 V	100.4100
C2,C3	C:	Fxd varmica 3.5 -13pF 5% 500V	108.0130
CR46,CR47,CR53,CR54, CR60,CR61,CR67,CR68, CR74,CR75,CR81,CR82, CR88,CR89,CR90,CR91	CR:	Switching (BA244)	133.0244
J1 thru J5, J11 thru J14, J21 thru J24, J31	Conn:	P.C. .156 10P	350.1004
J6,J9,J16,J17,J18,J19	Conn:	P.C. .125 15 Pos DR ST	350.3001
J27	Conn:	Ter 14 Pin Dil st 14P	354.0031
J60	Conn:	Ter 50 Pin Dil st 50P	354.0021
L1,L12,L13	L:	Fxd 250 mH Hi-Curr	150.1251
L2,L10,L11	L:	Fxd .33 UHY ±10%	150.8332
L3 thru L9	L:	Fxd 5.6 UHY	150.9562
R11, R13	R:	Fxd cflm 100 Ohm 5% 1/4W	116.1101
R12	R:	Fxd cflm 68 Ohm 5% 1/4W	116.0681
R19	R:	Fxd 220 Ohm 5% 1/4W	116.1221
R20	R:	Fxd 10 K Ohm 5% 1/4W	116.3101
R21	R:	Fxd 100 Ohm 5% 1/4W	116.1101

LTR	ECO NO	CHANGED BY	APPVD BY	DATE
A	PROTO	RELEASE		
B	1203	M MCM		
C	1226	L. PEND.		
D	1232	TR 7-22-81		
E	249	TR 11-16-81		
F	ECO A			



SHEETS 2,3 & 4 ARE A SIZE L/M

ROCKLAND
Rockland Systems Corporation

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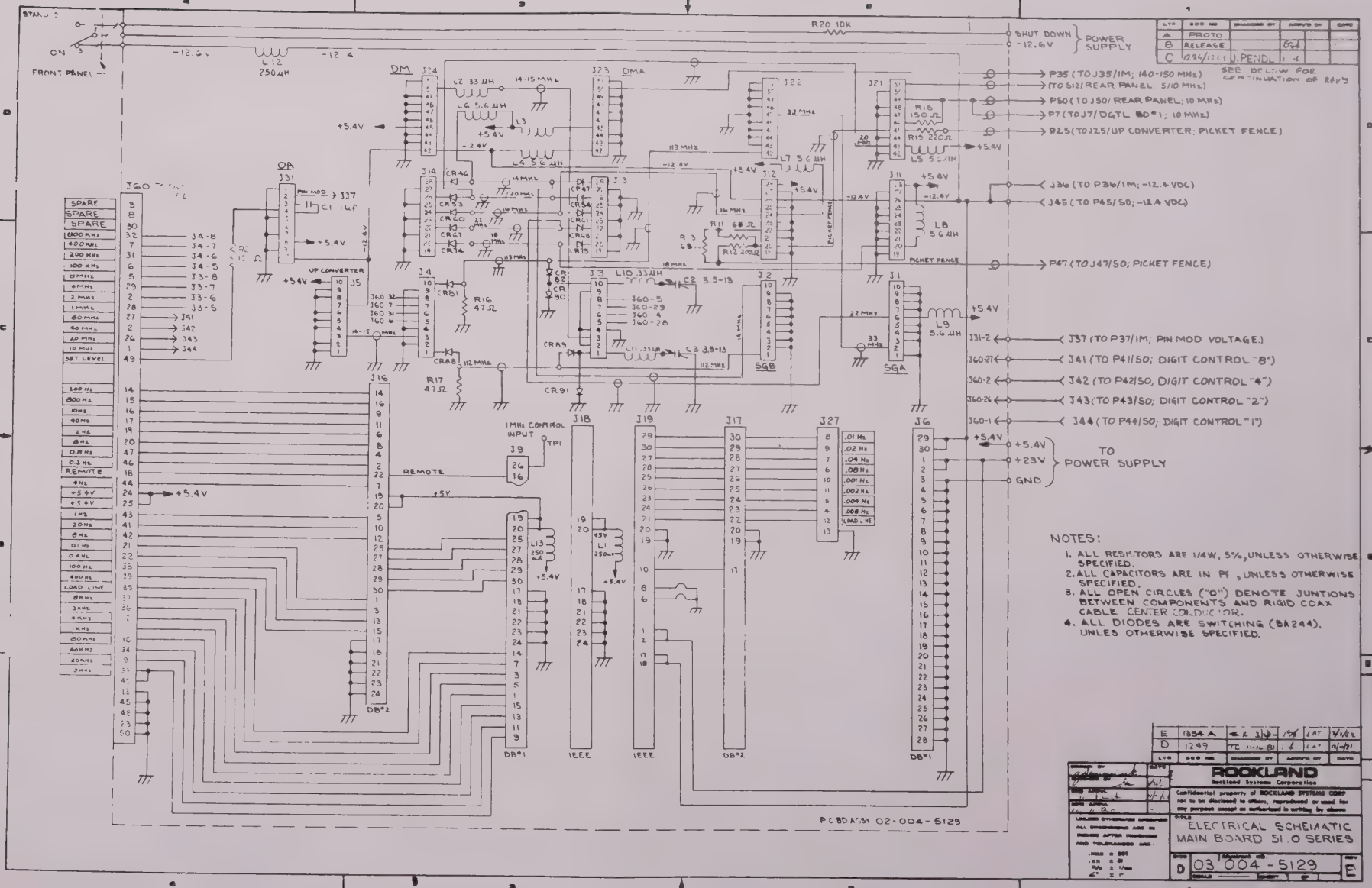
P.C. ASSEMBLY
MAIN BOARD SERIES

D 02 004-5129 F


SHUT DOWN
-12.6V
POWER SUPPLY
R20 10K
P35 (TO J35/1M; 140-150 MHz)
(TO S12/REAR PANEL: 5/10 MHz)
P50 (TO J50/REAR PANEL: 10 MHz)
P7 (TO J7/DGTL BD#1; 10 MHz)
P25 (TO J25/UP CONVERTER: PICKET FENCE)
SEE BELOW FOR CONTINUATION OF REVS
A PROTO
B RELEASE
C 1226/1211 J. PENDL
J36 (TO P36/1M; -12.4 VDC)
J45 (TO P45/50; -12.4 VDC)
P47 (TO J47/50; PICKET FENCE)
J37 (TO P37/1M; PIN MOD VOLTAGE)
J41 (TO P41/50; DIGIT CONTROL "8")
J42 (TO P42/50, DIGIT CONTROL "4")
J43 (TO P43/50; DIGIT CONTROL "2")
J44 (TO P44/50; DIGIT CONTROL "1")
+5.4V
+23V
GND
TO POWER SUPPLY
FRONT PANEL
ON
-12.6 V
-12.4
L12 250 µH
DM
DMA
J24
J23
J22
J21
J20
J14
J12
J11
J10
J4
J3
J2
J1
J60
J31
J5
J16
J9
J18
J19
J17
J27
J6
SGA
SGB
QA
UP CONVERTER
PIN MOD
REMOTE
1MHz CONTROL INPUT
PICKET FENCE
DB#1
DB#2
IEEE
SPARE
SET LEVEL
L2 33 µH
L3 1 µH
L4 5.6 µH
L7 5.6 µH
L8 5.6 µH
L9 5.6 µH
L10 33 µH
L11 33 µH
L13 250 µH
R16 47Ω
R17 47Ω
R18 150Ω
R19 220Ω
R11 68Ω
R12 270Ω
C2 3.5-13
C3 3.5-13
CR81
CR88
CR89
CR90
CR91
CR46
CR47
CR48
CR49
CR50
CR51
CR52
CR53
CR54
CR55
CR56
CR57
CR58
CR59
CR60
CR61
CR62
CR63
CR64
CR65
CR66
CR67
CR68
CR69
CR70
CR71
CR72
CR73
CR74
CR75
360-5
360-29
360-4
360-28
.01 Hz
.02 Hz
.04 Hz
.08 Hz
.001 Hz
.002 Hz
.004 Hz
.008 Hz
LOAD - HZ
200 KHz
400 KHz
200 KHz
100 KHz
80 MHz
60 MHz
40 MHz
20 MHz
10 MHz
8 MHz
4 MHz
2 MHz
1 MHz
800 KHz
400 KHz
200 KHz
100 KHz
80 KHz
40 KHz
20 KHz
10 KHz
8 KHz
4 KHz
2 KHz
1 KHz
800 Hz
400 Hz
200 Hz
100 Hz
80 Hz
40 Hz
20 Hz
10 Hz
8 Hz
4 Hz
2 Hz
1 Hz
0.8 Hz
0.4 Hz
REMOTE
LOAD LINE
J31-8
J31-7
J31-6
J31-5
J31-4
J31-3
J31-2
J31-1
J41
J42
J43
J44
+5.4V
+5V
-12.4V
PCB DASH 02-004-5129
NOTES:
1. ALL RESISTORS ARE 1/4W, 5%, UNLESS OTHERWISE SPECIFIED.
2. ALL CAPACITORS ARE IN PF, UNLESS OTHERWISE SPECIFIED.
3. ALL OPEN CIRCLES ("O") DENOTE JUNTIONS BETWEEN COMPONENTS AND RIGID COAX CABLE CENTER CONDUCTOR.
4. ALL DIODES ARE SWITCHING (BA244), UNLES OTHERWISE SPECIFIED.
E 1854 A
D 1249
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ELECTRICAL SCHEMATIC
MAIN BOARD 51.0 SERIES
D 03 004 - 5129 E

SECTION 5

MAINTENANCE, DIRECT DIGITAL SYNTHESIZER (DB1 and 2)
P/N's 004.5611 and 004.5612

5-1. INTRODUCTION

DB 1 and 2 are used to synthesize the final output digits from 0.001 Hz to the 10 KHz step. DB 2 generates a set of digital numbers corresponding to an analog sine wave for steps 100 Hz and below, while the other digits are generated digitally in DB 1. The two digital sine waves are combined in DB 1 and converted to an analog sine wave.

The boards mount in a card cage each using two connectors with asymmetric spacing assuring proper orientation. They are held in place by the connectors and the instrument's top cover resting on the ejectors mounted on the board.

5-2. PRINCIPLES OF OPERATION

The block diagram of Fig. 3-1 shows the DB 1 and 2 as part of the FINE RESOLUTION SECTION. Decades from 1 mHz through 10 KHz are generated in the DB boards and are added to a 1 MHz carrier frequency producing a signal between 1 and 2 MHz. In a later stage, the DM will add the 100 KHz decade, in effect shifting the digits from DB1 below 100 KHz one decade to the right. Therefore, if the synthesizer's output frequency is to be XYZ.876543210 MHz, then the output of DB 1 will be 1.76543210 KHz.

Fig. 5-1 shows the block diagram of the Digital Board. The frequency setting data in BCD format comes from the front panel or through the remote controls. These settings, as discussed above, will be one-tenth the actual frequency input to the DB boards. They are converted to binary format, stored in a Frequency Register and then added to the phase accumulator at a 10 MHz rate. A sine table ROM converts the ouput of the phase accumulator to a sample of a sine wave which are then converted to analog form by a Digital-to-Analog Converter (DAC) and a smoothing Low Pass Filter (LPF) cutting off at approximately 4 MHz.

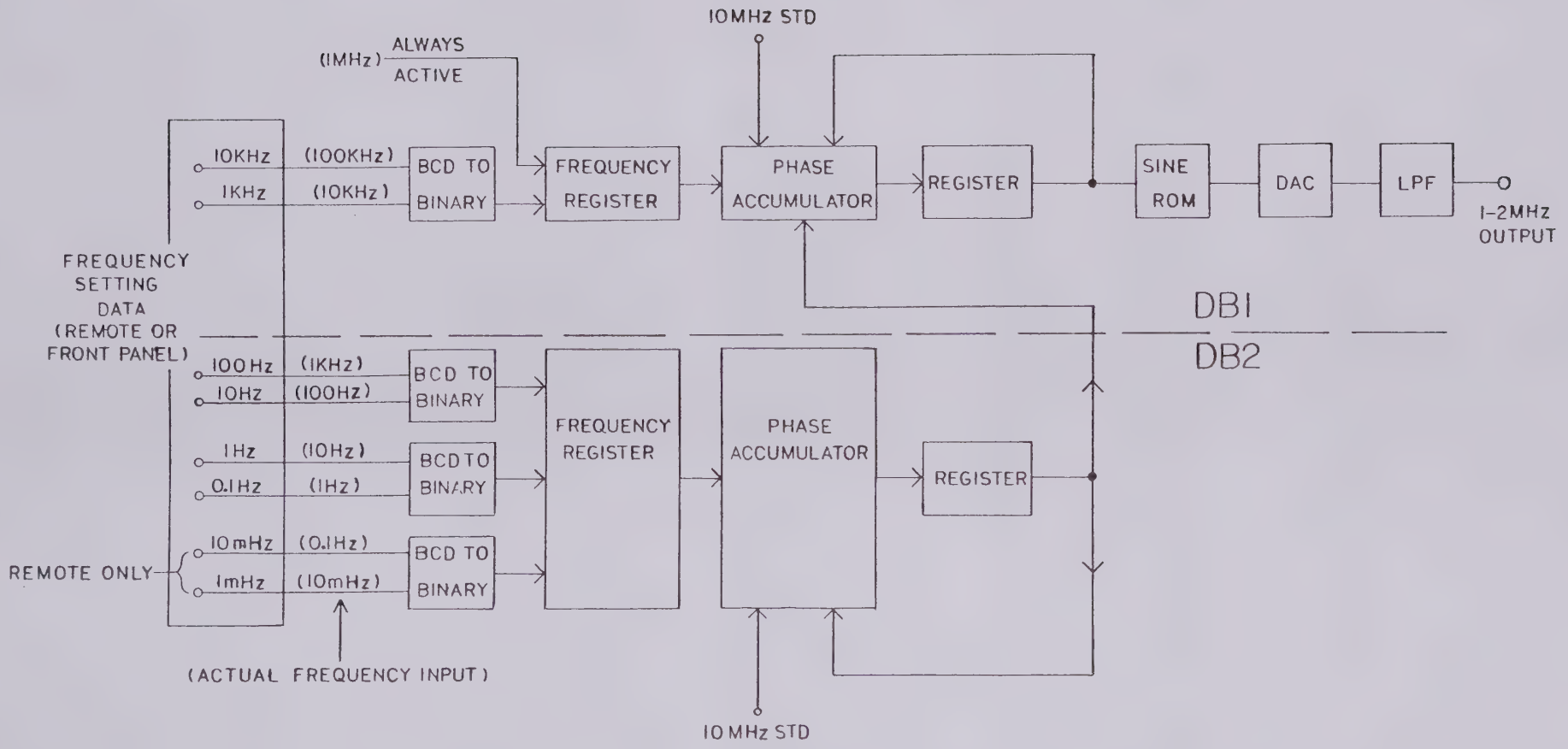


FIG. 5-1 BLOCK DIAGRAM OF THE DIGITAL BOARD (DB1 AND 2)

5-3. MODULE SPECIFICATIONS

Programming:	1, 2, 4, 8, BCD positive true High: 3.0 v minimum Low: 0.5 V maximum
Outputs (DB 1):	1 - 2 MHz
Spurious Outputs:	- 50 dB
Power:	5.4 V, 1000 ma -12.4 V, 25 ma 23 V, 120 ma

5-4. SERVICE

5-4-1. Maintenance

No preventive maintenance is required for either board. The presence of a correct output frequency and level indicates the modules are performing correctly.

Replacement of faulty components requires careful use of printed circuit repair techniques as applicable to double-sided boards with plated-through holes.

5-4-2. Alignment

Complete alignment of this module is made at the factory with a special test-set. Restoring the alignment of the analog sections after replacementoof individual parts in the field is not completely possible. The LPF (Low Pass Filter) may be aligned, while the rest may not.

5-4-3. Troubleshooting Procedure

Verify that a problem exists with Digital Board 1 or 2 by viewing the output of Digital Board 1 on a spectrum analyzer. Disconnect J8 (SMA connector) of Digital Board 1 and connect the output of Digital Board 1 to an analyzer with a 50 Ohm input impedance. The ouput should be a sine wave approximately - 16 dBm with harmonics down - 50 dBc. The frequency should be 1 MHz when the 10 KHz digit and lower are set to zero. Each step of the 10 KHz digit increases the output frequency 100 KHz. When all nines are set on the 10 KHz and lower digits the output frequency should be 2 MHz. If the correct output is not present, the following procedure will then isolate the problem to either Digital Board 1 or 2.

Check to see that power is supplied to both boards. Power is labeled on the printed circuit mainboard that the cards plug in to. Verify the presence of +23 V labeled on the mainboard near J8. Check for +5 V labeled near L1, and -12.4 V on pins 29 and 30 of J6. A 10 MHz standard signal must also be present for proper operation of the boards (see Fig. 5-1). Presence of this signal can be checked on the rear panel labeled "10 MHZ OUT" and on an "SMA

TYPE" connector J17 on Digital Board 1. Be sure to remove the shorts on J16 Pin 29 and 30 before inserting Digital Board 2.

Isolate the faulty board by removing Digital Board 2. Digital Board 2 plugs into J16 and J17. Connect a jumper from J16 Pins 29 and 30 to ground on the mainboard. Turn the synthesizer on and verify that the unit operates properly with digits 1 KHz and higher. If the unit operates properly, the problem must be Digital Board 2. If the problem still exists, replace Digital Board 1.

SECTION 6

MAINTENANCE, UPCONVERTER
P/N 004.5610

6-1. INTRODUCTION

The Upconverter is used to translate the 1 - 2 MHz output from Digital Board 1 to between 14 and 15 MHz for use as an input to the DM.

The module is of plug-in design and uses one ten-pin connector. It is secured with three 6-32 screws from the bottom of the deck. Housed in a frame and U - cover enclosure, the Upconverter can be removed as a complete unit after releasing the 6-32 panhead screws. The printed circuit board may also be removed separately from the enclosure, after the four cover screws (4-40) on top have been released and the cover has been lifted off.

6-2. PRINCIPLES OF OPERATION

Fig. 6-1 shows the Block Diagram of the Upconverter to the output of the DB1, 13 MHz is added in the Mixer. The 13 MHz LO is derived by filtering out 130 MHz from the 10 MHz count and dividing by ten.

6-2-1. Operation

Fig. 6-1 shows the Block Diagram of the Upconverter. 13 MHz is added in a Mixer to the output of Digital Board 1. The 13 MHz Local Oscillator is derived by filtering 130 MHz from the 10 MHz comb by dividing by ten. The output of the Mixer is filtered to remove the 13 MHz "LO" and translated harmonics of the Digital Board 1 output. The output frequency is 14 MHz for settings of all zeroes on the 10 KHz digit and below and 15 MHz for all nines on these digits.

6-2-2. Alignment

Complete alignment of this module is made at the factory with a special test-set, however replacement of semiconductors does not usually necessitate the alignment of tuned circuits. If the board does require realignment, return the module to the factory for adjustment.

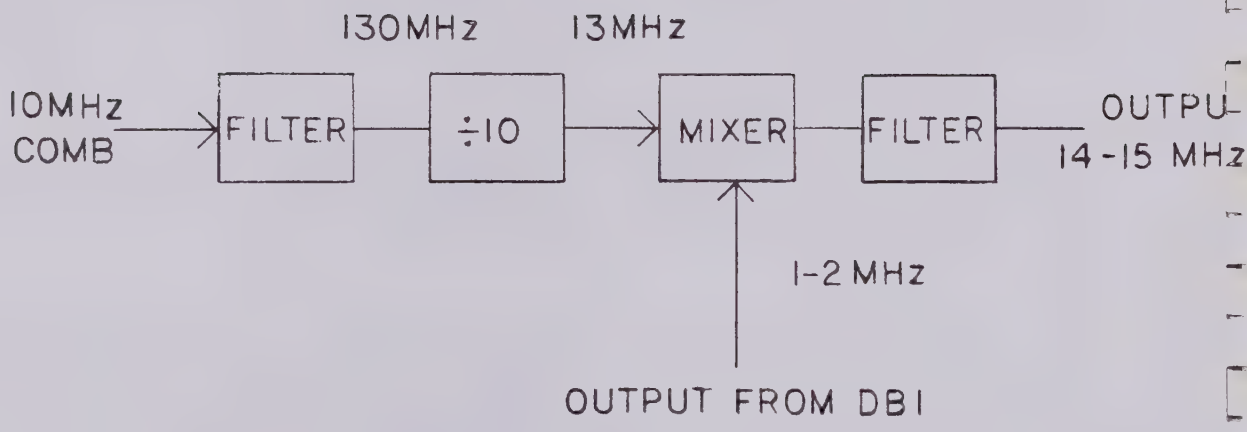


Fig. 6-1 Block Diagram Upconverter

SECTION 7

MAINTENANCE, DIGIT MODULE (DM)
P/N 002.5165

7-1. INTRODUCTION

The DM is used to synthesize, according to external command, the 100 KHz step.

The module combines analog, VHF and digital techniques. It is programmed through card-edge connectors with multiple low-inductance grounds provided for the RF signals.

The digit module is of plug-in design and uses three ten-pin connectors with asymmetric spacing assuring proper orientation; it is secured with three 6 - 32 screws from the bottom of the deck. Housed in a frame and U - cover enclosure, the DM can be removed as a complete unit after releasing the 6 - 32 panhead screws. The printed circuit board may also be removed separately from the enclosure, after the four cover screws (4-40) on top have been released and the cover has been lifted off. Holes near the top corners of the board facilitiate prying the board up and free of the connectors by using a small tool alternately on both sides.

7-2. PRINCIPLES OF OPERATION

The Block Diagram of Fig. 7-1 shows the DM receiving the output signal from the Upconverter. Its frequency is between 14 and 15 MHz. The output of the DM will also be between 14 and 15 MHz.

The DM module has the following arithmetic capabilities: when receiving a frequency of 14.xyz...MHz from the Upconverter, it will produce an output frequency of 14.axyz...MHz, where "a" directly corresponds to the 100 KHz dial setting (digit control) of the module. In other words, all digits behind the decimal point are moved to the right by one position (reduced in significance by ten), and a 100 KHz step, as selected by the digit control (manual or remote), is placed ahead of the received digits.

Fig. 7-1 is a block diagram of the DM module. Apart from the input and output, the module is connected to the following fixed bus frequencies: 112 MHz, 113 MHz, 14, 16, 18, 20, 22 MHz, which are all crystal-oscillator-derived and coherent. For any one digit selection, the DM uses either 112 or 113 MHz and one of the five lower frequencies. 112 or 113 MHz is used to make even or odd digits respectively; 14 MHz is used with digits 0, 1; 16 MHz is used with digits 2, 3; 18 MHz with digits 4, 5, and so on.

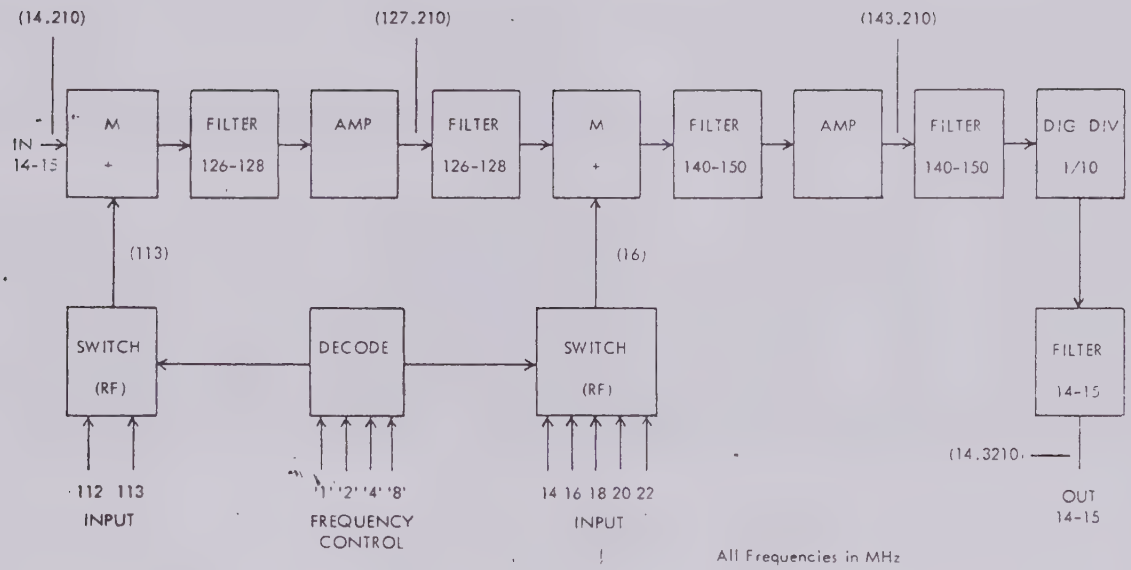


Fig. 7-1 Block Diagram, DM Module

To illustrate the operation, the block diagram shows as an example all frequencies which are internally produced in a DM, if it receives an input of 14.210 MHz and the 100 KHz digit is set to "3". With the aid of the DM Schematic Diagram, the circuitry used to effect the arithmetic may be traced.

The 14.210 MHz input as received on pin 3 is fed to the base of Q10, an additive mixer. Digit control pins 5 and 6 (weight 1 and 2) are "high" if a "3" is selected, and decoder - IC's U1 and U2 furnish two DC outputs: "3" being odd, Q2, the 113 MHz switch, is turned on; and since "3" belongs to the second pair of ten frequencies (2, 3), Q5, which controls 16 MHz, is turned on.

The 113 MHz signal reaches the base of Q10 via C28. The upper sideband (sum) of the two inputs to Q10, 14.210 MHz and 113 MHz, is 127.210 MHz. Two double-tuned filters and amplifier Q11, which have passband of 126 - 128 Mhz, deliver this frequency to the input of the second mixer Q8/Q9.

Transformer T1 is connected to the output of switch-transistors Q3 to Q7, and, since Q5 is turned on, 16 MHz is the other input to the second mixer. Again, the circuits following are tuned to select the upper sideband, which is between 140 and 150 MHz. Our specific example signal is 127.210 MHz plus 16 MHz, or 143,210 MHz. The filters suppress the lower sideband and other unwanted products. After amplification, the signal reaches U3, which is a digital divide-by-ten IC. The output is filtered by a tuned circuit and a signal of 14.3210 is fed to pin 50. As we see, a "3" has been placed ahead of "210", and the latter digits have moved one position to the right.

7-3. MODULE SPECIFICATIONS

Inputs:	14 - 15 MHz	0.20 - 0.35 V
	112, 113 MHz	0.10 - 0.17 V
	14, 16, 18, 20, 22 MHz	90 - 125 mV
Output:	14 - 15 MHz	0.25 - 0.31 V Nominal 0.20 V Minimum Load: 1.3 K Ohms in parallel with 30 pF
Programming:	1, 2, 4, 8 BCD, positive true	
	High: 3.0 V Minimum	Low: 0.5 V Maximum
Spurious Outputs:	- 75 dB	
Power:	+5.4 V, 100 mA $\pm$ 10%	-12.4 V, 38 mA $\pm$ 10%

7-4. SERVICE

7-4-1. Maintenance

No preventive maintenance is required for the DM. The presence of an output signal of correct frequency and level indicates that the module is operating

properly. The output of the module is produced directly by an IC divider. A 10 dB window exists at the divider input, and minor aging effects will, therefore, not impair operation.

Replacement of faulty components requires careful use of printed-circuit repair techniques as applicable to double-sided boards with plated-through holes.

7-4-2. Alignment

Complete alignment of this module is made at the factory with a special test-set. Restoring the alignment after replacement of individual parts in the field is possible. It is recommended that voltages given in the Troubleshooting Procedure be used and that, in general, touch-up alignment be performed only on those tuned circuits which may have been altered by the parts replacements. Replacement of semiconductors will not necessitate realignment of tuned circuits in general.

7-4-3. Troubleshooting Procedure

Section 4 of this manual provides information to isolate faulty modules. It is important to follow the procedures given in detail to ensure that all the common supply frequencies are present before attempting to repair modules.

If the DM module has been isolated as faulty, the preferred service mode is exchange and factory repair. When immediate service is needed, the following procedure may be used.

Test Equipment Required:

RF Voltmeter	1 - 300 MHz, 10 mV - 1 V, High Impedance Probe (3 pF, DC Res. 100 K Ohms)
HF Counter	0 - 200 MHz, 10 mV Sensitivity, High Impedance or 50 Ohm Input

The output of the DM module is on pin 50, which is also the test point designation used in Section 4 and the running number of the board-edge connector as shown on the Schematic and Assembly drawings. The module produces 14.000 MHz at a level of 0.2 - 0.35 V into the DMA module if all instrument dials have been set to zero. As the 100 KHz dial is changed through successive numbers 0 to 9, the output frequency should change in 100 KHz steps from 14.000 MHz to 14.900 MHz. If the output is of the proper frequency but low in level, the output tank L10/C62 or the tuning should be checked. C62 is peaked at a setting of 5 (14.500 MHz). Only the voltmeter probe must remain connected to pin 50 for final tuning.

Absence of output for some dial settings points to specific causes:

1. No output on two successive even-odd digits (e.g. 2, 3) indicates that the second mixer, Q8, Q9 does not receive one of the

low bus frequencies from 14 to 22 MHz, and the fault is likely located in the switch section (Q3 to Q7). 14 MHz is used for digit 0, 1; 16 MHz for digit 2, 3, and so on.

2. No output on either all odd or all even digits will result from failure in the 112/113 MHz switches Q1 or Q2, since 112 MHz is used to produce the even digits and 113 MHz to make the odd digits.

3. If no output is obtained on any digit, if random digits are missing, or if an unsteady counter reading (noise) is present, the divider (U3) is faulty or the input on pin 7 is low. 0.2 V minimum is to be read at this point with only the voltmeter connected. If the above checks (1 and 2) were positive, then part of the circuitry that is used on all digits is faulty. The active devices are Q10, Q11, Q8, Q9 and Q12. DC operating conditions on all these transistors are such that 1.1 to 1.5 V should be measured across their emitter resistors R40, R45, R34 and R48.

RF voltages at various stages are given to permit further localization of the trouble. The previously indicated level of 0.2 V into pin 7 of the divider is a minimum; other voltages may differ from normal by + 3 dB.

Base Q10:	0.10 V
Base Q11:	0.05 V
C23/C24:	0.50 V
Base Q12:	0.07 V
U3, Pin 7:	0.28 V

The 126 - 128 MHz signal at C23/C24 peaks at digit setting "5" and drops approximately 2 dB for settings "0" and "9" on the preceding DM module (less significant digit). Voltage at pin 7 of U3 responds to digit settings on the DM under test, and the minimum voltage must be obtained for all settings.

REPLACEABLE PARTS LIST

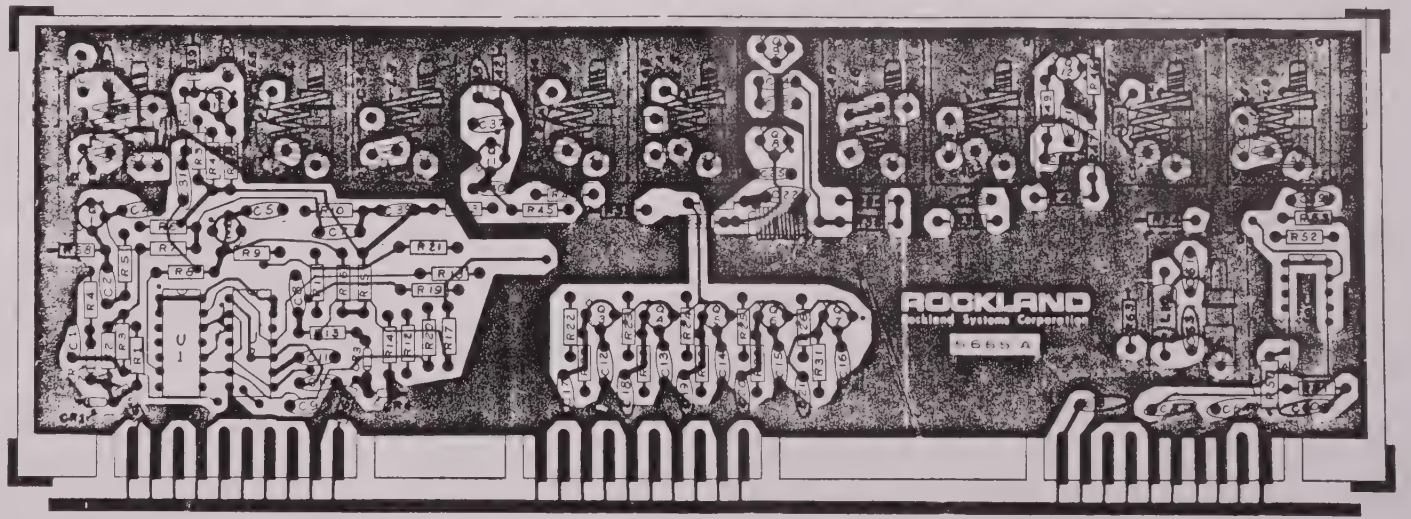
PC BD ASSEMBLY, DM MODULE
P/N 004.5165

Ref. Des.		Description	P/N
C1,C4,C5,C9, C10,C11,C12,C13, C14,C15,C16	C:	Fxd cer .001 uF 10% 500V X5F	100-2105
C2,C8,C17,C18, C19,C20,C21	C:	Fxd cer 220 pF 10% 500 V X5F	100.1225
C3,C6,C7,C60	C:	Fxd cer .05 uF 20% 25 V Y5P	100.3501
C22,C64	C:	Fxd cer 68 pF 5% 500 V N750	100.0687
C23,C34,C32,C35, C41,C45	C:	Fxd cer 22 pF 5% 500 V NPO	100.0229
C25,C29,C30,C39, C40,C52,C53	C:	Fxd cer .01 uF +80 -20% 50 V Z5V	100.3101
C26	C:	Fxd cer 27 pF 5% 500 V NPO	100.0279
C28,C37,C38,C51	C:	Fxd cer 5.0 pF 500 V NPO	100.9509
C31	C:	Fxd cer 47 pF 5% 500 V NPO	100.0479
C34,C43	C:	Fxd cer .68 pF ± .25 pF 500 V NPO	106.8689
C46	C:	Fxd cer 15 pF 5% 500 V NPO	100.0159
C48	C:	Fxd cer 3.3 pF ± .5 pF 500 V NPO	100.9339
C49,C54,C57,C59, C51,C63	C:	Fxd cer 10 pF 5% 500 V NPO	100.0109
C56	C:	Fxd cer 2.2 pF 500 V NPO	100.9229
C62	C:	Var mica 1.2 - 10 pF 5% 500 V	108.0100
CR1,CR2,CR3,CR4	CR:	Switching (BA244)	133.0244
CR5,CR6	CR:	SL LW LK 70 PIV	132.4151
(L1 C27),(L2 C33), (L4 C42),(L5 C44), (L6 C47),(L7 C50), (L8 C55),(L9 C58)	Tuned Ckt Assy: 5600		012.7401
(L3 C36)	Tuned Ckt Assy: "DM" Module		012.7407
L10	L:	Fxd 5.6 uH 10%	150.9562
Q1,Q2,Q3,Q4, Q5,Q6,Q7	Q:	Sil PNP (2N3250)	136.3250
Q8,Q9,Q10	Q:	Sil NPN (2N2369)	134.2369
Q11,Q12	Q:	Sil NPN (2N5179)	134.5179
R1,R7,R15	R:	Fxd cflm 10 K Ohm 5% 1/4W	116.3101
R2,R10,R16,R58	R:	Fxd cflm 2.2 K Ohm 5% 1/4W	116.2221
R3,R8,R36,R44, R55,R56	R:	Fxd cflm 15 Ohm 5% 1/4W	116.0151
R4,R9,R14,R37	R:	Fxd cflm 680 Ohm 5% 1/4W	116.1681
R5,R12,R13,R32	R:	Fxd cflm 47 Ohm 5% 1/4W	116.0471
R6,R11,R22,R23, R24,R25,R26,R62	R:	Fxd cflm 1.0 K Ohm 5% 1/4W	116.2101

Replaceable Parts List DM Module P/N 004.5165 Continued

Ref. Des		Description	P/N
R17,R18,R19,R20, R21,R35,R38,R43, R47	R:	Fxd cflm 1.5 K Ohm 5% 1/4W	116.2151
R27,R28,R29,R30, R31,R40	R:	Fxd cflm 330 Ohm 5% 1/4W	116.1331
R33,R39,R42,R46	R:	Fxd cflm 6.8 K Ohm 5% 1/4W	116.2681
R34	R:	Fxd cflm 220 Ohm 5% 1/4W	116.1221
R45,R48	R:	Fxd cflm 150 Ohm 5% 1/4W	116.1151
R49,R51	R:	Fxd cflm 4.7 Ohm 5% 1/4W	116.9471
R50	R:	Fxd mflm 2.21 K Ohm 1% 1/8W	111.2210
R52	R:	Fxd cflm 680 Ohm 5% 1/4W	116.1686
R53,R54,R63	R:	Fxd cflm 470 Ohm 5% 1/4W	116.1471
R57	R:	Fxd cflm 33 Ohm 5% 1/4W	116.0331
R59,R60,R61	R:	Fxd cflm 100 Ohm 5% 1/4W	116.1101
T1	Transformer Assy: 5600		012.7301
U1	U:	Dual 4-IN NAND Gate	121.7420
U2	U:	Quad 2-IN NAND Gate	121.7400
U3	U:	Bi-Quinary Ctr (MC10138)	127.0138

LTR	ECO NO	CHANGED BY	APPV'D BY	DATE
A	REL		BOH JV	5/19/82



SHEETS 2, 3 & 4 ARE "A" SIZE P/L

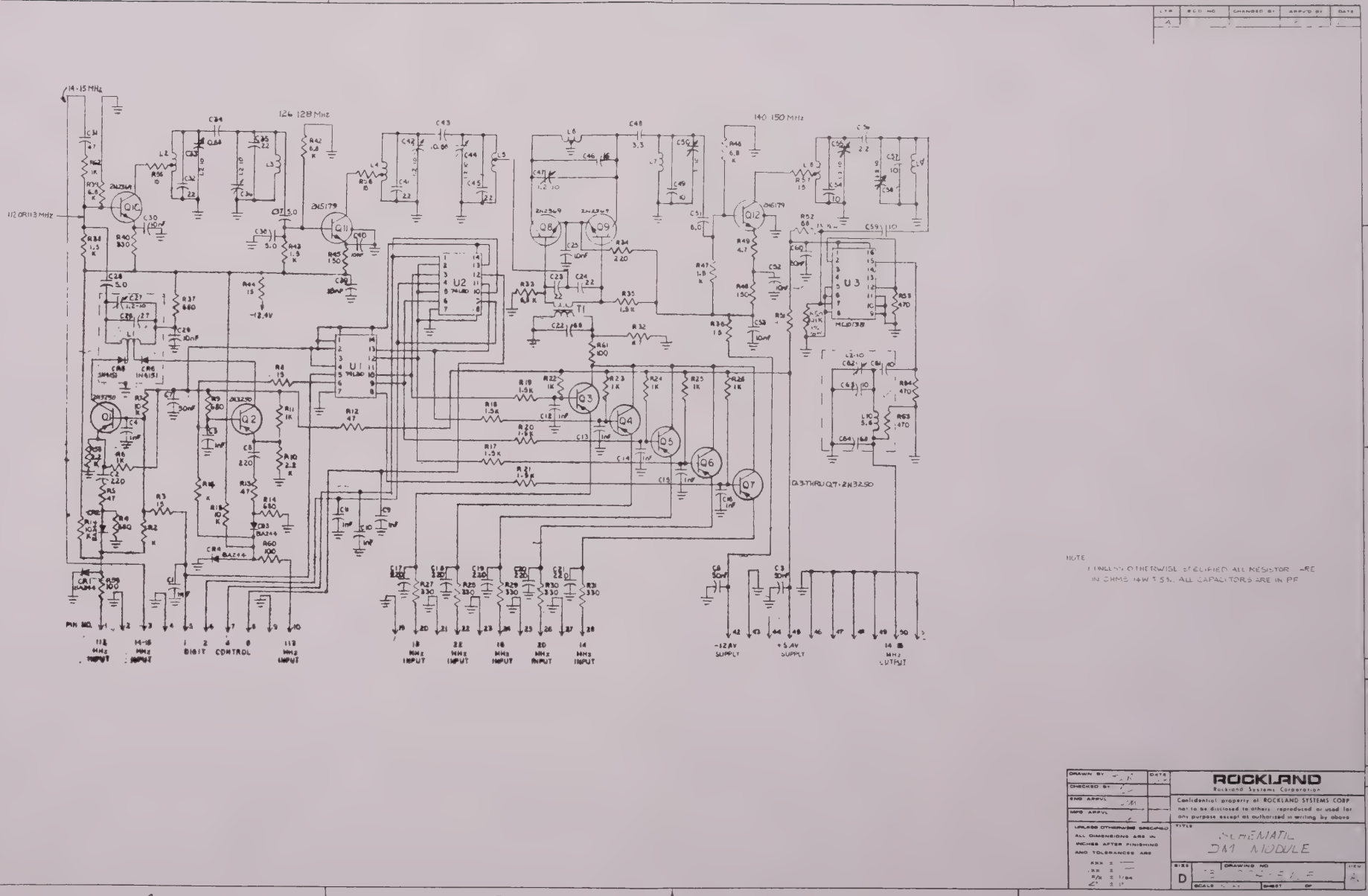
DRAWN BY S.R	5/19/82	ROCKLAND Rockland Systems Corporation
CHECKED BY		Confidential property of ROCKLAND SYSTEMS CORP. not to be disclosed to others, reproduced or used for any purpose except as authorized in writing by above.
ENG APPVL BOH	5/19/82	
MFG APPVL. JV	6/1/82	

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AFTER FINISHING AND TOLERANCES ARE:
.XXX ± .005
.XX ± .01
X/X ± 1/64
∠° ± 1°

TITLE: P.C. BD. ASSEMBLY, DM MODULE 5130720

SIZE	DRAWING NO	REV
C	02 004 5165	A

SCALE 2/1 SHEET 1 OF 4



NOTE
UNLESS OTHERWISE SPECIFIED ALL RESISTOR ARE IN OHMS 1/4W 5%. ALL CAPACITORS ARE IN PF

LTR	ECO NO	CHANGED BY	APPVD BY	DATE
A				

DRAWN BY		DATE
CHECKED BY		
ENG APPVL		
MFG APPVL		

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AFTER FINISHING AND TOLERANCES ARE
XXX ±
XX ±
F/X ± 1/64
ANG ± 1°

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TITLE
SCHEMATIC
DM MODULE

SIZE	DRAWING NO	REV
D	[illegible]	A
SCALE	SHEET	OF

SECTION 8

MAINTENANCE, DIGIT MODULE A (DMA)
P/N 002.5150

8-1. INTRODUCTION

The Digit Module A (DMA) generates the 1 MHz steps. It is very similar to the DM module and is fed by the DM. Its output at 140 - 150 MHz contains the 1 MHz steps and all finer steps, down to 0.001 Hz.

This section should be seen as supplemental and must be used in conjunction with the DM portion.

The digit module is of plug-in design and uses three 10 pin connectors with asymmetric spacing assuring proper orientation; it is secured with three 6 - 32 screws from the bottom of the deck. Housed in a frame and U-cover enclosure, the DMA can be removed as a complete unit after releasing the 6 - 32 panhead screws. To gain access to the PC board, the 4 - 40 top screws and all 2 - 56 side screws must be removed from the module U-cover. The PC board cannot be removed without first removing the module from the deck.

8-2. PRINCIPLES OF OPERATION

The main difference between the DM and DMA modules is the absence of the final division-by-ten in the DMA. As a result, the arithmetic function of the DMA can be described as follows:

When receiving a frequency of 14.xyz from the preceding DM, it will produce an output frequency of 14 A.xyz MHz, where A directly corresponds to the DMA dial setting. In other words, all digits behind the decimal point are retained, and a 1 MHz step, as selected by the digit control (manual or remote) is placed ahead of the received digits.

All other observations made in the DM Principles of Operation apply here as well, and the frequency shown in the block diagram (Fig. 3-1) at the output of the DMA, namely 146.876543210, would be obtained if the DMA had been instructed to produce a "6" digit.

Apart from the absence of the final divider, there are additional components used in the execution of the 14 to 22 MHz selection switch. This added, switched selectivity removes unwanted frequencies before they can enter the balanced mixer. These frequencies are not attenuated by division or a narrow-band output as they are in the DM module. All input levels to the DMA are identical with the levels for the DM modules. The output level of the DMA, however, at 140 - 150 MHz is +2 to +6 dBm into a 50 Ohm load. This module feeds the mixer in the IM module through a 50 Ohm pad.

8-3. SERVICE

8-3-1. Maintenance

No preventive maintenance is required for DMA modules. The presence of an output signal of correct frequency and level indicates that the module is operating properly. The output of the module is included in the leveling loop, and minor aging effects will, therefore, not impair operation.

Replacement of faulty components requires careful use of printed-circuit repair techniques as applicable to double-sided boards with plated-through holes.

8-3-2. Alignment

Complete alignment of this module is made at the factory with a special test-set. Restoring the alignment after replacement of individual parts in the field is possible. It is recommended that voltages given in the Troubleshooting Procedure be used and that, in general, touch-up alignment be performed only on those tuned circuits which may have been altered by the parts replacements. Replacement of semiconductors will not necessitate realignment of tuned circuits in general.

8-3-3. Troubleshooting Procedure

Section 4 of this manual provides information to isolate faulty modules. It is important to follow the procedures given in detail to ensure that all the common supply frequencies are present before attempting to repair modules.

If a DMA module has been isolated as faulty, the preferred service mode is exchange and factory repair. When immediate service is needed, the following procedure may be used.

Test Equipment Required:

RF Voltmeter	1 - 300 MHz, 10 mV - 1 V, High Impedance Probe (3 pF, DC Res. 100 K Ohms)
HF Counter	0 - 200 MHz, 10 mV Sensitivity, High Impedance or 50 Ohm Input

The output of the DMA module is on pin 50, which is also the test point designation used in Section 4 and the running number of the board-edge connector as shown in the Schematic and Assembly Drawings. The module produces 140.000 MHz at a level of +2 to +6 dBm into the IM module if all instrument dials have been set to zero. As the dial of the DMA module is changed through successive numbers 0 to 9, the output frequency should change in 1 MHz steps from 140.000 MHz to 149.000 MHz. If the output is of the proper frequency but low in level, the fault is in the 14 - 22 MHz switch, the mixer (Q8, Q9), or the 140 - 150 MHz output filters L6 to L10 and transistor Q12. Alignment of

this section cannot be restored in the field, but active devices are generally replaceable without need for realignment. See DC operation conditions listed below.

Absence of output for some dial settings points to specific causes:

1. No output on two successive even-odd digits (e.g. 2,3) indicates that the second mixer, Q8, Q9 does not receive one of the low bus frequencies from 14 to 22 Mhz, and the fault is likely located in the switch section (Q3 to Q7). 14 MHz is used for digit 0, 1; 16 MHz for digit 2, 3; and so on.

2. No output on either all odd or all even digits will result from failure in the 112/113 MHz switches Q1 or Q2, since 112 MHz is used to produce the even digits and 113 MHz to make the odd digits.

3. If no output is obtained on any digit, if random digits are missing, or if an unsteady counter reading (noise) is present, part of the circuitry that is used on all digits is faulty. The active devices are Q10, Q11, Q8, Q9 and Q12. DC operating conditions on all these transistors are such that 1.1 to 1.5 V should be measured across their emitter resistors R40, R45, R34 and R48. Bases of switch transistors Q3 to Q7 are at +5.2 V when inactive, at +3.3 V when turned on.

RF voltages at various stages are given to permit further localization of the trouble. Voltages may differ from nominal by + 3 dB.

Base Q10:	0.10 V
Base Q11:	0.05 V
C23/C24:	0.50 V
Base Q12:	0.07 V

The 126 - 128 MHz signal at C23/C24 peaks at digit setting "5" and drops approximately 2 dB for settings "0" and "9" on the preceding DM module (less significant digit).

REPLACEABLE PARTS LIST

PC BD ASSEMBLY, DMA MODULE
P/N 004.5150

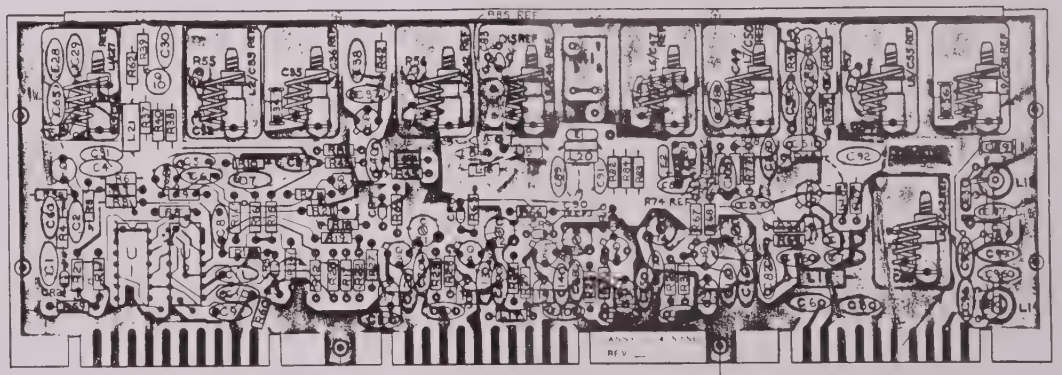
Ref. Des.		Description	P/N
C1,C4,C5,C9, C10,C11,C12,C13, C14,C15,C16	C:	Fxd cer .001 uF 10% 500 V X5F	100.2105
C2,C8,C77	C:	Fxd cer 220 pF 10% 500 V X5F	100.1225
C3,C6,C7,C25, C29,C30,C39,C40, C52,C53	C:	Fxd cer .01 uF +80 -20% 100 C	100.3104
C17,C18,C19,C20, C21,C23,C24,C31, C60,C61	C:	Fxd cer 47 pF 5% 500 V NPO	100.0479
C26,C76	C:	Fxd cer 27 pF 5% 500 V NPO	100.0279
C28,C37,C51,C69	C:	Fxd cer 5.0 pF + .25 pF 500 V NPO	100.9509
C32,C35,C41,C45	C:	Fxd cer 22 pF 5% 500 V NPO	100.0229
C34,C43	C:	Fxd cer .68 pF + .25 pF 500 V NPO	106.8689
C38,C70	C:	Fxd cer 33 pF 5% 500 V NPO	100.0339
C46,C67	C:	Fxd cer 15 pF 5% 500 V NPO	100.0159
C48	C:	Fxd cer 3.3 pF + .5 pF 500 V NPO	100.9339
C49	C:	Fxd cer 10 pF 5% 500 V NPO	100.0109
C54,C57,C63	C:	Fxd cer 12 pF 5% 500 V NPO	100.0129
C56,C59	C:	Fxd cer 1.5 pF + .25 pF NPO	106.9159
C64,C71,C72,C73, C74,C75	C:	Var mica 3.5 - 13 pF 5% 500 V	108.0130
C65	C:	Fxd cer 2.2 pF + .5 pF 500 V NPO	100.9229
C66	C:	Fxd cer 91 pF 5% 500 V N750	100.0917
C68	C:	Fxd cer 56 pF 5% 500 V NPO	100.0569
C78	C:	Fxd cer 100 pF 10% 500 V X5F	100.1105
CR2,CR3,CR7,CR8, CR9,CR10,CR11	CR:	Switching (BA244)	133.0244
CR5,CR6	CR:	Sil Cmptr 75 PIV (1N4151)	132.4151
(L1 C27),(L2 C33), (L3 C36),(L4 C42), (L5 C44),(L6 C47), (L7 C50),(L8 C55), (L9 C58),(L10 C62)	Tuned Ckt Assy: 5600		012.7401
L11	L:	Fxd 1.0 uH + 5%	150.9102
L12	L:	Fxd .33 uH + 10%	150.8332
Q1,Q2	Q:	Sil PNP (2SA711)	137.0711
Q3,Q4,Q5,Q6,Q7	Q:	Sil PNP (2N3250)	136.3250
Q8,Q9,Q10	Q:	Sil NPN (2N2369)	134.2369
Q11,Q12	Q:	Sil NPN (2N5179)	134.5179

Replaceable Parts List DMA Module P/N 004.5150 Continued

Ref. Des.		Description	P/N
R1,R7,R15	R:	Fxd cflm 10 K Ohm 5% 1/4W	116.3101
R2,R10,R16,R58	R:	Fxd cflm 2.2 K Ohm 5% 1/4W	116.2221
R3,R8,R36,R44, R55,R56,R57	R:	Fxd cflm 15 Ohm 5% 1/4W	116.0151
R4,R9,R14,R37, R50	R:	Fxd cflm 680 Ohm 5% 1/4W	116.1681
R5,R12,R13,R32	R:	Fxd cflm 47 Ohm 5% 1/4W	116.0471
R6,R11,R21,R22, R23,R24,R25, R26,R62	R:	Fxd cflm 1.0 K Ohm 5% 1/4W	116.2101
R17,R18,R19,R20, R35,R38,R43,R47	R:	Fxd cflm 1.5 K Ohm 5% 1/4W	116.2151
R27,R28	R:	Fxd cflm 560 Ohm 5% 1/4W	116.1561
R29,R30,R31	R:	Fxd cflm 470 Ohm 5% 1/4W	116.1471
R33,R39,R42,R46	R:	Fxd cflm 6.8 K Ohm 5% 1/4W	116.2681
R34	R:	Fxd cflm 68 Ohm 5% 1/4W	116.0681
R40	R:	Fxd cflm 330 Ohm 5% 1/4W	116.1331
R45,R48	R:	Fxd cflm 150 Ohm 5% 1/4W	116.1151
R49	R:	Fxd cflm 4.7 Ohm 5% 1/4W	116.9471
R59,R60	R:	Fxd cflm 100 Ohm 5% 1/4W	116.1101
R63	R:	Var cmt 500 Ohm 1/4 Rnd	118.1502
R64,R65,R66,R67, R68	R:	Fxd cflm 22 K Ohm 5% 1/4W	116.3221
R69	R:	Fxd cflm 220 Ohm 5% 1/4W	116.1221
T1	Transformer Assy: 5600		012.7301
U1	U:	Quad 4-IN NAND Gate	121.7420
U2	U:	Quad 2-IN NAND Gate	121.7400

SEE ECO 1194 & 1237

ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY		DATE
	A	RELEASE				
	B		M.M			
	C	1277	DP			
	D	1331	DP			
	E	1351				
	F	1390				
	G	1423				
	H	1427				
	J	1451				
	K	1483				
	L	1495				



TAP PLACEMENT CHART		
COIL	TURNS	TAP WITH
L1	2.0	CR6 CATHOD
L1	2.25	CR5 CATHOD
L2	1.5	R55
L4	1.5	R56
L5	.25	C83
L6	1.75	BUSS TO GND
L8	3.5	R57
L10	.75	BUSS TO PAD

SHEETS 2,3,& 4 ARE "A" SIZE L/M

DR	DATE 12-22-81
CHKD	
ENG	
MFG	
ISSUED	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE

WAVETEK ROCKLAND Wavetek Rockland, Inc

P.C. ASSEMBLY
DMA MODULE

SIZE	MODEL NO	DRAWING NO	REV
D	5130/20	02-004-5150	L

SCALE 2:1 CODE IDENT 23338 SHEET 1 OF 4

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ZONE	LTR	ECO NO	CHANGED BY	APPRVD BY	DATE
	A	RELEASE			
	B	1194 & 1237	JP		
	C	1277	M. MCMAHON		
	D	1322	DP		
	E	1331	DP	RR LAT	1-11-82
	F	1350	MP 8/25/82	LJ CM	11/8/82
	G	1423	MP 8/3/82	LJ CM	8/10/82
	H	1451	RP 8/24/82	LJ CM	9/8/82
	J	1483	DP 11/5/82	LJ SK	11/5/82
	K	1495	CM 11/8/82	LJ SK	11/8/82

NOTE:
1. UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE IN OHMS, ¼ WATT ± 5%, ALL CAPACITORS ARE IN PF.
2. NOMINAL VALUE, SELECT AT TEST AS REQUIRED.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK ROCKLAND	Wavetek Rockland, Inc.
MATERIAL	DRAWN M. MCMAHON 10/23/81	TITLE	ELECTRICAL SCHEMATIC DMA MODULE
FINISH	CHKD		
	ENG APPR R R 11/19/82		
	MFG APPR LAT 1-11-82		
	ISSUED	SIZE D	MODEL NO 5130/2003 DRAWING NO 004-5150 REV K
		SCALE NONE	CODE IDENT 23338 SHEET 1 OF 1

SECTION 9

MAINTENANCE, STANDARD GENERATORS (SGA, SGB)
P/N 002.5640, P/N 002.5645

9-1. INTRODUCTION

The SGA and SGB are standard generators used in the Wavetek Rockland Model 5130A Synthesizer. They operate together from a crystal-oscillator input and, by direct arithmetic operations, produce common supply frequencies. These standard frequencies are distributed in the deck and used by most other modules in the synthesizer.

The SGA module can operate from either 5 or 10 MHz, and with this input, it produces discrete frequencies of 18, 20, 22 and 33 MHz on separate outputs and all harmonics of 10 MHz from 10 to 140 MHz with equal amplitude on one output. These frequencies are used by the SGB, DM's, DMA and SO modules in the synthesis process.

The SGB receives the 10 to 140 MHz picket fence from the SGA module and produces 14 and 16 MHz, 112 and 113 MHz, all on separate outputs. These frequencies are used by the DM's and DMA modules.

The SGA and SGB modules use DC power at +5.4 V and -12.4 V. Since the outputs are constant and not subject to selection or control, no programming inputs are provided. These modules combine analog, VHF and digital techniques. All inputs and outputs are fed through card-edge connectors with multiple grounds provided for the RF signals.

These modules are unique; they are not interchangeable with any other module in the synthesizer. Both units are of plug-in design using three 10 pin connectors with asymmetric spacing, which assure proper orientation.

They are secured with three 6 - 32 panhead screws from the bottom of the deck. Housed in a frame and U-cover enclosure, the SGA and SGB can be removed after releasing the three 6 - 32 screws. To gain access to the PC boards, the 4 - 40 top screws and 2 - 56 screws have to be removed from the module U-cover. Printed circuit boards cannot be removed without first removing the modules from the deck.

9-2. PRINCIPLES OF OPERATION

The SGA and SGB standard generators which operate together, are depicted in the Block Diagram of Fig. 9-1.

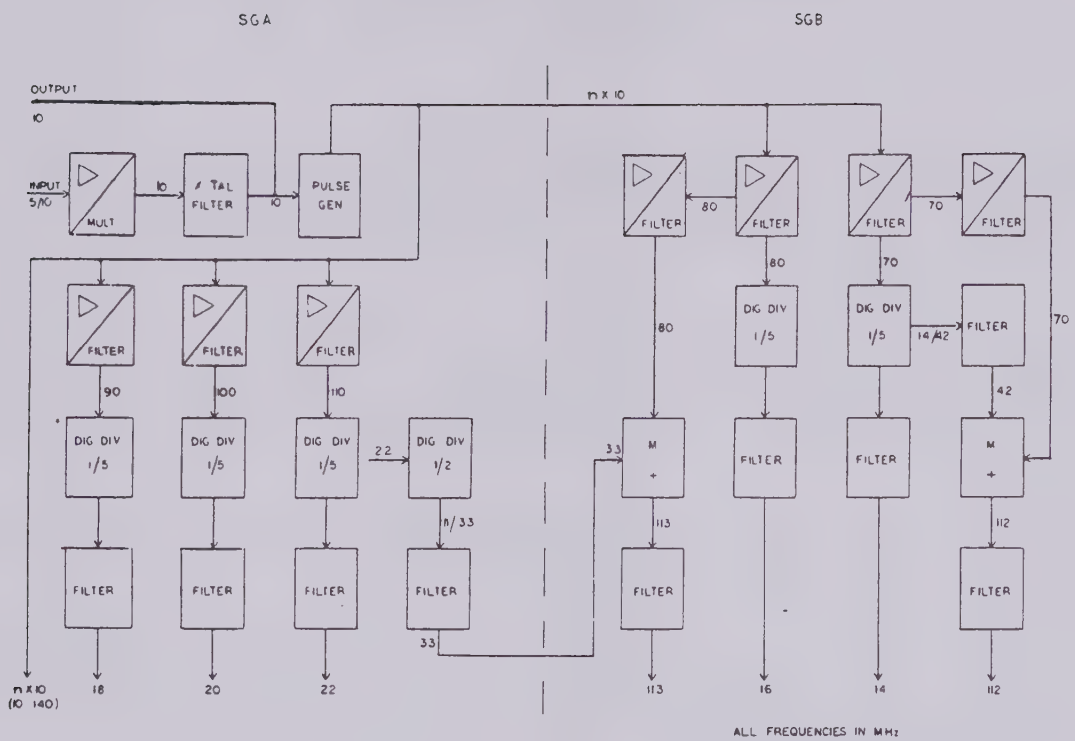

Fig. 9-1 Block Diagram, SGA & SGB Modules

An input of 5 or 10 MHz at a level of 0.4 V is received from an external or internal frequency standard and fed to the input amplifier/multiplier. This block is followed by a narrow crystal filter. The pulse generator receives its input from this crystal filter and produces a spectrum which is the basis for all fixed or standard frequencies in the synthesizer. Of these, the five low frequencies of 14, 16, 18, 20 and 22 MHz are produced by division of a specific spectrum line through an amplifier-filter circuit, a digital divider, and a filter at the output frequency. The two higher standard frequencies of 112 and 113 MHz also use one specific spectrum line each. Mixers (M) add derivatives of certain low standard frequencies, as shown, to obtain the final frequencies. Thus, by multiplication, division and addition, the SGA and SGB produce seven standard frequencies which are completely coherent with the input frequency of 5 or 10 MHz.

As shown in the SGA Schematic Diagram, the 5 or 10 MHz input signal drives Q7, which amplifies or multiplies, and a 10 MHz single-pole crystal filter Y1 follows, which removes noise (and attenuates 5 MHz). The resulting 10 MHz signal can be used externally (to drive slave instruments) from the output of emitter-follower Q6. It is applied internally to pulse generator Q5/Q4.

At the output of the pulse generator (R23/R24) a spectrum of n x 10 MHz multiples from 10 to 140 MHz is available. These frequencies are the source of all standard frequencies in the instrument. Three of the lower frequencies are produced in the SGA.

Since the three sections are identical, a description of one - the 20 MHz generator - will suffice to illustrate the process. Loosely coupled to the spectrum bus by C16, transistor Q3 amplifies the 100 MHz line, and this signal, after filtering in L16, C17, C18, reaches the divider U3. The divide-by-five section of U3 is used, and a 20 MHz signal from pin 4 is connected to a tuned circuit. A low impedance output, taken across C35, is fed to the 20 MHz bus in the deck.

A frequency of 33 MHz is needed to produce 113 MHz in the SGB module. This signal is produced by U1, where the 22 MHz output is divided by 2 and the third harmonic, after filtering, is fed to pin 2 and then to the SGB module.

As shown on the SGB Schematic Diagram, the SGB receives the 10 to 140 MHz spectrum from the SGA module on pin 20. The schematic shows, starting from the middle, on the left-hand side the generation of 14 MHz and 112 MHz signals, and in the right half the generation of 16 MHz and 113 MHz. The low frequencies are produced by the same divide-by-five process which is used in the SGA module: the 70 MHz line is pre-filtered, amplified and filtered in L4, C13, C14 from where it enters divider U1; the resulting 14 MHz signal, after filtering, reaches pin 10, the output.

The same IC also supplies a third harmonic of 14 MHz to Q3. After amplification this 42 MHz signal serves as injection to Q1, which is the final mixer to produce 112 MHz by adding a 70 MHz input from Q2.

The 16 MHz generation is identical to the 14 MHz circuits, and 80 MHz is filtered and amplified further to drive mixer Q7 on the 113 MHz side. The 33

MHz signal, coming from the SGA, is amplified in Q8 and then fed to the mixer. Double-tuned filters are employed on both sides to filter the 112 and 113 MHz mixer outputs.

9-3. SERVICE

9-3-1. Maintenance

No preventive maintenance is required for the SGA or SGB modules. The presence of standard output signals of correct frequency and level indicates that the modules are operating properly.

All outputs of the SGA and SGB modules, with the exception of the 112 and 113 MHz signals, are produced directly by IC digital dividers. A 10 dB window exists at the divider inputs and minor aging effects will, therefore, not impair operation.

Replacement of faulty components requires careful use of PC repair techniques as applicable to double-sided boards with plated-through holes.

9-3-2. Alignment

Complete alignment of these modules is made at the factory with a special test set. Restoring the alignment after replacement of individual parts in the field is possible. It is recommended that voltages given in the Troubleshooting Procedure be used, and that in general touch-up alignment be performed only on those tuned circuits which may have been altered by the parts replacements. Replacement of semiconductors will not necessitate realignment of tuned circuits in general.

9-3-3. Troubleshooting Procedure

Section 4 of this manual provides information necessary to isolate faulty modules. It is important to follow the procedures step by step to ensure proper identification of failure before attempting to repair modules.

If an SGA or SGB module has been isolated as faulty, the preferred service mode is exchange and factory repair. When immediate service is needed, the following procedure may be used.

Test Equipment Required:

RF Voltmeter	1 - 300 MHz, 10 mV, High Impedance Probe (3 pF, DC Res. 100 K Ohms)
HF Counter	0 - 200 MHz, 10 mV Sensitivity, High Impedance or 50 Ohm Input
Spectrum Analyzer	10 - 600 MHz, 50 Ohm Input, 60 dB min. dynamic range, Resolution 1 MHz

Section 4, Troubleshooting, isolates failures in the SGA and SGB to specific outputs. In addition, the Block Diagram (Fig. 9-1) and Schematic Diagrams are structured such that individual circuit-sections are recognizable, and this will aid in the search for the failure.

DC checks of suspected active devices are the proper first step. Voltage drops across the emitter resistors of the transistors are all 1.2 - 1.5 V, except in the SGA across R36 and R25, where 1.9 - 2.3 V are normal (R25 with RF drive).

Basic to all output signals is the presence of the picket fence of 10 - 140 MHz. The spectrum analyzer connected in place of the SO module (J1) must show each frequency with a level of -16 to -9 dBm.

The active devices in the pulse generator are Q7, Q5 and Q4. Crystal-filter Y1 output is 0.4 - 0.5 V across R31.

If the picket fence is normal, low level or absence of a specific frequency may be traced as follows: connect the SA to the output in question. Total absence of output in a 14 to 22 MHz frequency generally indicates that the divider is not triggered. All injection voltages, which are connected to pin 7 of the IC (MC - 10138), are accessible to the Voltmeter probe from the component side of the board. A minimum level of 0.3 V is required there. The input and output trimmer capacitors may be identified and retuned (e.g., the trimmers for the 90 MHz circuits feeding the 18 MHz divider are C10 and C12).

If a specific low frequency (14 to 22 MHz) is displayed on the SA, but the level is low, output circuits are defective or detuned. Every output circuit is tuned by a single trimmer (e.g., C42 tunes the 18 MHz output).

The 112 and 113 MHz outputs are the result of mixing two frequencies. In both cases the first step in troubleshooting is to check the 14 or 16 MHz outputs as detailed before. If these low frequencies are present, connect the SA to the faulty output (112 or 113 MHz) and attempt to tune: C9, C29, C4, C1 for the 112 MHz output and C46, C53, C56, C60 for the 113 MHz output. At the bases of Q1 and Q7, 0.4 V minimum should be obtained; this is a composite of both injections. This level and its variation with tuning both injections will locate the fault in either one of the mixer inputs or the output circuits following the mixer.

REPLACEABLE PARTS LIST

PC BD ASSEMBLY, SGA MODULE
P/N 004.5640

Ref. Des		Description	P/N
C1,C7,C8,C14, C20,C22,C23,C28, C32,C33,C34,C53, C54	C:	Fxd cer .01 uF +80 -20% 50 V Z5V	100.3101
C2,C9,C15	C:	Fxd cer 22 pF 5% 500 V NPO	100.0229
C3,C10,C19,C21, C31,C36,C42,C46, C49	C:	Var mica 3.5 - 13 pF 5% 500 V	108.0130
C4,C11,C16	C:	Fxd cer 1.0 pF ± .25 pF 500 V NPO	106.9109
C6	C:	Fxd cer 27 pF 5% 500 V NPO	100.0279
C13	C:	Fxd cer 47 pF 5% 500 V NPO	100.0479
C18,C29	C:	Fxd cer 33 pF 5% 500 V NPO	100.0339
C24	C:	Fxd cer 100 pF 10% 500 V X5F	100.1105
C25	C:	Mica dp 110 pF 5% 500 V	101.1110
C26	C:	Var mica 1.2 - 10 pF 5% 500 V	108.0100
C27	C:	Fxd tant 6.8 uF 20% 16 V	109.5680
C30	C:	Fxd cer 120 pF 10% 500 V X5F	100.1125
C35,C41,C45	C:	Fxd cer .001 uF 10% 500 V X5F	100.2105
C37,C38,C39,C44,C52	C:	Fxd cer .05 uF +80 -20% Z5V	100.3502
C40,C43,C47,C48,C55	C:	Fxd cer 5.0 pF ± .25 pF 500 V NPO	100.9509
C50	C:	Fxd cer 10 pF 5% 500 V NPO	100.0109
C51	C:	Fxd cer 560 pF 10% 500 V X5F	100.1565
CR1	CR:	Sil Cmptr 75 PIV (1N4151)	132.4151
L1,L2,L3	L:	Fxd .33 uH ± 10%	150.8332
L4	L:	Air Inc .20 uH Nom	012.1002
L5	L:	Fxd 2.2 uH ± 5%	150.9222
L6	L:	Fxd 1.0 uH ± 5%	150.9102
L7,L9,L11	L:	Fxd 22 uH ± 10%	150.0222
L8,L10,L12,L13	L:	Fxd 5.6 uH ± 10%	150.9562
(L14 C5),(L15 C12), (L16 C17)	Tuned Ckt Assy: 5600		012.7403
Q1,Q2,Q3,Q4	Q:	Sil NPN (2N5179)	134.5179
Q5	Q:	Sil PNP (2N3250)	136.3250
Q6,Q7	Q:	Sil NPN (2N2369)	134.2369
R1,R4,R7,R30,R37	R:	Fxd cflm 6.8 K Ohm 5% 1/4W	116.2681
R2,R5,R8,R40	R:	Fxd cflm 330 Ohm 5% 1/4W	116.1331
R3,R6,R9,R34,R38	R:	Fxd cflm 1.5 K Ohm 5% 1/4W	116.2151
R10,R15,R19,R35	R:	Fxd cflm 2.2 K Ohm 5% 1/4W	116.2221
R11,R12,R13,R17,R21	R:	Fxd cflm 220 Ohm 5% 1/4W	116.1221

Replaceable Parts List PC BD Assembly SGA Module P/N 004.5640 Continued

Ref. Des.	Description	P/N
R14,R16,R18,R29	R: Fxd cflm 680 Ohm 5% 1/4W	116.1681
R20,R22,R24,R33, R43,R44	R: Fxd cflm 15 Ohm 5% 1/4W	116.0151
R23,R28,R36,R42	R: Fxd cflm 100 Ohm 5% 1/4W	116.1101
R25,R26	R: Fxd cflm 1.0 K Ohm 5% 1/4W	116.2101
R27	R: Fxd cflm 4.7 K Ohm 5% 1/4W	116.2471
R31	R: Fxd cflm 68 Ohm 5% 1/4W	116.0681
R32,R39,R41	R: Fxd cflm 47 Ohm 5% 1/4W	116.0471
U1,U2,U3	U: Bi-Qinary Cntr (MC10138)	127.0138
Y1	Filter: Crystal 10 MHz	165.3005

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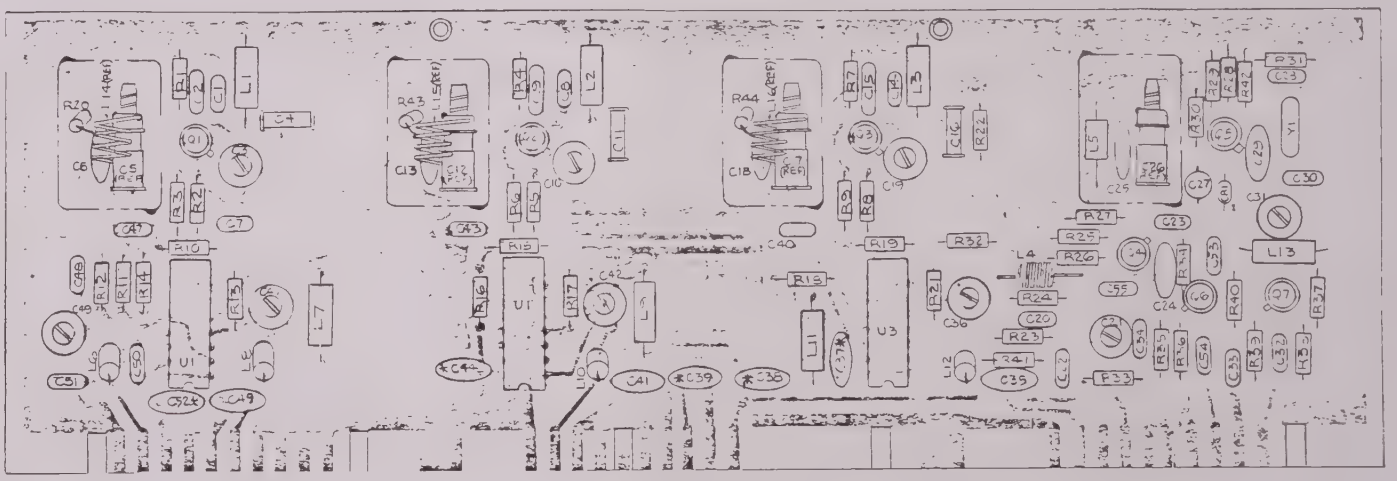
ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE

x/x	xxx	xx	∠
± 1/64	± .005	± .01	± 1°

MATERIAL

FINISH

DO NOT SCALE DWG
REMOVE ALL BURRS
BREAK SHARP EDGES

	DATE
DRAWN	
CHKD	
ENG APPR.	
MFG APPR	
ISSUED	

WAVETEK ROCKLAND — Wavetek Rockland, Inc.

TITLE: P.C.B. ASSY SGA MODULE

SIZE	DWG DEL NO	DRAWING NO	REV
C	5/30/20	02-004-5640	B

SCALE | CODE IDENT 23338 | SHEET | OF

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ZONE	LTR	ECO NO	CHANGED BY	APPRVD BY	DATE
	A	RELEASE		LAH	LAT	5/4/81
	B	1279	TR 10/13/81	LAH	LAT	10/14/81

PICKET FENCE (10-140 MHz)

NOTES

1) UNLESS OTHERWISE SPECIFIED:
- ALL RESISTORS ARE IN OHMS, 1/4 W, ±5%.
- ALL CAPACITORS ARE IN PF.
- ALL INDUCTORS ARE, IF SPECIFIED, IN UH.

2) TYP FOR MC10138

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE: .XX ±.02, .XXX ±.005, ANGLES ±.5°. MATERIAL: FINISH.

DO NOT SCALE DWG. REMOVE ALL BURRS. BREAK SHARP EDGES.

DRAWN TR 10/13/81 | CHKD | ENG APPR. | MFG APPR. Lewis A Tatum 11-9-81 | ISSUED

WAVETEK ROCKLAND — Wavetek Rockland, Inc.

TITLE: ELECTRICAL SCHEMATIC SGA MODULE

SIZE D | MODEL NO. 5130/20 | DRAWING NO. 03-009-5640 | REV B

SCALE — | CODE 23338 | SHEET 1 OF 1

REPLACEABLE PARTS LIST

PC BD ASSEMBLY, SGB MODULE
P/N 004.5645

Ref. Des.	Description	P/N
C2,C3,C20,C41, C57,C59	C: Fxd cer 33 pF 5% 500 V NPO	100.0339
C5,C58	C: Fxd cer 0.5 pF ± .25 pF 500 V NPO	106.8509
C6,C38,C48	C: Fxd cer 22 pF 5% 500 V NPO	100.0229
C7,C35	C: Fxd cer 2.2 pF 5% 500 V NPO	100.9229
C8	C: Mica dp 56 pF 5% 500 V	101.0560
C10,C15,C17,C21, C29,C39,C45,C50, C51,C55	C: Fxd cer .01 uF +80 -20% 50 V Z5V	100.3101
C11,C43	C: Fxd cer 10 pF 5% 500 V NPO	100.0109
C12,C32	C: Fxd cer 1.5 pF ± .25 pF NPO	106.9159
C13,C37,C47,C54	C: Fxd cer 47 pF 5% 500 V NPO	100.0479
C16,C42,C44,C49	C: Fxd cer 2.2 pF ± .5 pF 500 V NPO	100.9229
C18,C61	C: Fxd cer 27 pF 5% 500 V NPO	100.0279
C19,C26,C31,C36, C53,C62	C: Var mica 3.5-13 pF 5% 500 V	108.0130
C22	C: Fxd cer 15 pF 5% 500 V NPO	100.0159
C23	C: Fxd cer 560 pF 10% 500 V X5F	100.1565
C24,C63	C: Fxd cer 12 pF 5% 500 V NPO	100.0129
C25	C: Fxd cer 5.0 pF ± .25 pF 500 V NPO	100.9509
C27,C64	C: Fxd cer .0015 uF 10% 500 V X5F	100.2155
C28,C33,C34,C52,C66	C: Fxd cer .05 uF +80 -20% Z5V	100.3502
C30	C: Fxd cer 6.8 pF ± .25 pF NPO	106.9689
C65	C: Fxd cer .001 uF 10% 500 V X5F	100.2105
(L1 C1),(L2 C4), (L7 C56),(L8 C60)	Tuned Ckt Assy: 5600	012.7401
(L3 C9),(L4 C14), (L5 C40)	Tuned Ckt Assy: 5600	012.7402
(L6 C46)	Tuned Ckt Assy: "SGB" Module	012.7408
L9,L11,L12,L16	L: Fxd .33 uH ± 10%	150.8332
L10,L13	L: Fxd 5.6 uH ± 10%	150.9562
L14,L15	L: Fxd 22 uH ± 10%	150.0222
L17	L: Fxd 1.0 uH ± 10%	150.9100
Q1,Q2,Q3,Q4, Q5,Q6,Q7,Q8	Q: Sil NPN (2N5179)	134.5179
R1,R24,R28	R: Fxd cflm 150 Ohm 5% 1/4W	116.1151
R2,R5,R11,R16,R19, R27,R29,R32	R: Fxd cflm 1.5 K Ohm 5% 1/4W	116.2151
R3,R6,R7,R17,R18, R30,R33,R34	R: Fxd cflm 6.8 K Ohm 5% 1/4W	116.2681
R4	R: Fxd cflm 330 Ohm 5% 1/4W	116.1331

Replaceable Parts List PC BD Assembly SGB Module P/N 004.5645 Continued

Ref. Des.		Description	P/N
R8	R:	Fxd cflm 470 Ohm 5% 1/4W	116.1471
R9,R12,R22,R26	R:	Fxd cflm 680 Ohm 5% 1/4W	116.1681
R10,R21	R:	Fxd cflm 2.2 K Ohm 5% 1/4W	116.2221
R13,R25,R35,R36, R37,R38,R39, R40,R41	R:	Fxd cflm 15 Ohm 5% 1/4W	116.0151
R14,R15,R20,R23, R31	R:	Fxd cflm 220 Ohm 5% 1/4W	116.1221
U1,U2	U:	Bi-Quinary Cntr (MC10138)	127.0138

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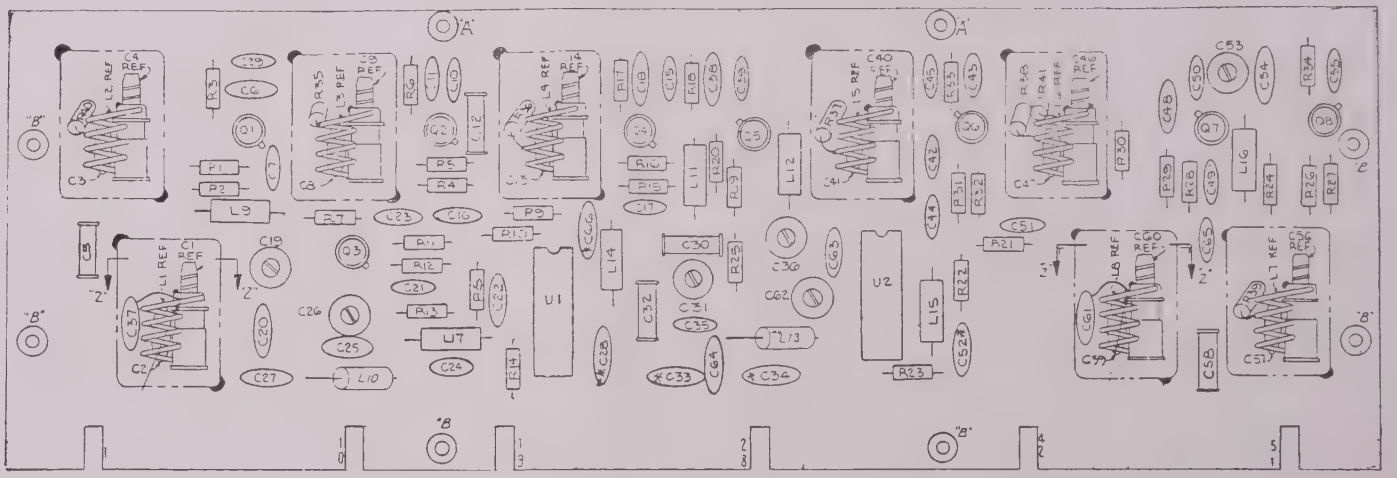

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK ROCKLAND Wavetek Rockland, Inc.
X/X ± 1/64 | .XXX ± .005 | .XX ± .01 | ∠ ± 1°	DRAWN / DATE	TITLE: PCB ASSY SGB MODULE
MATERIAL:	CHKD	
FINISH:	ENG APPR.	
	MFG APPR.	
	ISSUED	SIZE C | MODEL NO 5130/20 | DRAWING NO 02-004-5645 | REV B
		SCALE | CODE IDENT 23338 | SHEET OF

R.S. KRAFT

4 3 2 1

SECTION 10

MAINTENANCE, 10 MHz STEP SECTION
STEPPED OSCILLATOR (SO), P/N 002.5135
INTERMEDIATE MIXER (IM), P/N 002.5655
OUTPUT AMPLIFIER (OA), P/N 002.5660

10-1. INTRODUCTION

The 10 MHz Step Section consists of three separate modules, the SO, the IM and the OA. They work in conjunction with the 505 MHz bandpass filter as the final functional block of the 5130 Synthesizer. This block performs frequency translation to obtain the selected 10 MHz decade within the 160 MHz range and also provides the desired output level over a 10 dB range up to +13 dBm.

The heart of the 10 MHz Step Section is the Stepped Oscillator (SO) whose digitally controlled frequency spans a 150 MHz range in 10 MHz increments. Together with the Intermediate Mixer module (IM), it performs a drift-cancelled double-conversion process, which adds or subtracts the appropriate 10 MHz harmonic from the picket-fence to the signal supplied by the DMA module. The Output Amplifier (OA), brings the signal to a level of 20 mW. Level control is accomplished through a feedback loop involving a "PIN" diode modulator in the IM module as the variable gain element. The controlling signal is derived from a level-sensing detector and comparator in the OA module.

The modules of this section are unique, not interchangeable with each other or other modules in the synthesizer. All three modules employ coax connectors which must be released before removal from the deck is possible. In addition, the IM and SO modules use push-on connectors for various supply and programming inputs. The OA module uses one 10 pin card-edge connector. The modules are secured from the bottom of the deck by 6 - 32 panhead screws; the SO uses three, the OA and IM two each. The PC boards of these modules are not accessible without removal of the module from the deck and subsequent removal of the covers. The 505 MHz filter is permanently mounted to the deck structure.

10-2. PRINCIPLES OF OPERATION

The two main functions of the 10 MHz step section are:

1. Generation of the 10 MHz steps in the synthesis process.

2. Output amplification and level control.

With the aid of the Model 5130A Block Diagram (Fig. 3-1) and the Schematic Diagrams appearing at the end of this Section these functions will now be explained in greater detail.

10-2-1. The 10 MHz Step Function

In order to obtain the desired output frequency, a 10 MHz multiple must be added or subtracted from the 140 - 150 MHz signal provided by the DMA module. This is done in a drift-cancelled loop involving the SO and the IM modules and a narrow passband filter centered at 505 MHz. A major element in this scheme is the Stepped Oscillator in the SO module, which can be set to one of 16 frequencies at 10 MHz increments by a 4-bit control word.

The program input is hexadecimal code and the TTL level is first transposed by zener diodes CR1 thru CR4 by approximately -12 V. The 1-of-16 decoder (U1, U2, Q8) operates from -6.8 V to -11.4 V; the latter is a stabilized and filtered voltage, produced by regulator CR8, Q9/Q10, Q11. Stabilization and low ripple are needed since this voltage is eventually applied to the oscillator varactor diodes. The output of the decoder, by connecting one of the divider resistors R1 thru R16 to -11.4 V, produces proper voltages to set oscillator Q7 to frequencies from 365 MHz to 515 MHz in 10 MHz steps.

The oscillator frequency is changed by means of varactor diodes CR6 and CR7. Control voltage ranges from -1.9 V (365 MHz) to -11.0 V (515 MHz), approximately.

The oscillator output is fed to two separate three-stage amplifiers for gain and isolation; at both mixers M1 and M2 this signal is used as the swtiching (LO) signal with a level of +10 to +16 dBm. M1 is connected through an attenuator in the deck and a low-pass filter (L1, L2, L3 and capacitors) to the one of the sum or difference frequencies equals 505 MHz. This signal is CO filtered by the bandpass filter connected to J2. The output of the filter feeds the IM module.

Mixer M2 produces the instrument output signal, which is amplified in the OA module. The low level input to M2 at J4 (365 - 355 MHz), which carries all digits except the 10 MHz steps, comes from the IM module. Any frequency drift of the VCO affects the two inputs to M2 in the same direction and by the same amount; this cancels completely in the final output (0.1 to 160 MHz), which is the difference between the two mixer inputs.

The IM module contains the other elements of the drift-cancelled loop: a 505 MHz broadly tuned amplifier, a mixer, a pin-diode attenuator and a 3-pole bandpass filter centered at 355 - 365 MHz.

The unit receives a 505 MHz signal from the SO module via the 505 MHz bandpass filter located in the deck. Five-stage amplifier Q1 thru Q5 increases this signal to drive mixer M1 at approximately + 15 dBm.

The low level signal to M1 is the 140 - 150 MHz input which comes from the DMA through a matching pad. Mixer M1 produces 365 - 355 MHz, the difference between 505 MHz and 140 - 150 MHz. This signal is fed to the "PIN" modulator CR1 - CR4, which is driven from the OA and is part of the output levelling loop. Minimum attenuation is obtained with a -11.5 V input. The signal is then filtered in the 3-pole filter (L1, L2, L3) and fed back to the SO via J3, thereby closing the drift-cancelling loop.

10-2-2. Output Amplification and Level Control

The final output (0.1 - 160 MHz) from M2 in the SO module is a low-level signal of nominally -24 dBm. The output amplifier OA module provides the necessary wideband gain and levelling of amplitude to produce instrument outputs up to +13 dBm across the band from a 50 Ohm source-impedance with substantially flat response.

The RF gain portion from input J2 to output J1 provides insertion gain in a 50 Ohm system of approximately 40 dBm from 100 KHz to 160 MHz, if the "level set" voltage on pin 22 is 2.0 VDC. The four stage amplifier uses emitter degeneration at low frequencies to obtain a flat response. Two stages of preamplification are followed by a driver and a PNP - NPN push-pull output stage. The module input, which is connected to the final mixer output in the SO module, contains a matching pad and a low-pass filter to reduce levels of signals above 165 MHz.

Between the first and second stage a PIN-diode attenuator is used to effect a reduction in gain by some 8 dB for a "set level" voltage reduction from 2.0 V to 0.63 V. This reduces the overall loop gain without substantial loss of signal-to-noise ratio.

To operate the levelling loop, the RF output signal is detected by CR1/CR2. The resulting DC voltage, after suitable amplification, is compared to the "set Level" voltage in the differential pair Q9/Q10. The output of this amplifier through Q11 regulates the current of the PIN-diode attenuator in the IM module, which controls the amplifier input signal such that only a minute error-voltage exists between the "set level" voltage and the collector voltage of Q8. This means that the RF voltage at the detector is stabilized at a constant set level. The actual output voltage into a matched load impedance (50 Ohms) is one-half of the detector voltage with R26 providing the 50 Ohm source impedance.

10-3. SERVICE

10-3-1. Maintenance

No preventive maintenance is required for the three modules of this section. The presence of output signals of correct frequency and level indicates that the modules are operating properly. Minor aging effects will not impair performance. Detailed verification of systems and module operation is made with the system Troubleshooting Chart in the System Section (Section 4).

10-3-2. Alignment/Calibration

Modules are tested and calibrated at the factory in special test fixtures. Complete alignment of the SO and IM modules is beyond the scope of this manual; most active and passive components of these modules, however, can be replaced if they become defective, without any recalibration. The only calibration in the OA module is the level adjustment described below.

10-3-3. OA Module, Level Calibration

The OA module has a cover with holes for performing calibration and, therefore, it does not have to be removed. If the OA module has to be removed, proceed as follows: remove module from deck after carefully releasing coax connectors and 6-32 screws. Remove cover, reinstall module without cover, connect power or level meter (50 Ohm terminated) directly to the output jack. Set frequency to 100 MHz and front panel Level control fully clockwise; adjust R36 to obtain +13 dBm on power or level meter. Reset Level control fully counter clockwise (but not in indent position); adjust R41 to obtain +3 dBm reading on power meter. Repeat sequence several times to eliminate effect of interaction.

10-3-4. Troubleshooting

Section 4 of this manual has the necessary information to isolate a faulty module in the 10 MHz Step Section. It is important to follow the procedure in detail to ensure proper identification of the faulty module. Further tests here require the same test equipment as detailed under Section 4.

Aspects of the generation of the proper frequency are all covered in the Troubleshooting Chart (see Table 4-1). This leaves the checks concerning the levelling loop.

A normally functioning instrument will produce a PIN-modulator voltage (orange lead, OA pin 20) of -4 to -11.0 V at an output setting of +13 dBm into 50 Ohm load. This voltage (PIN voltage) is an easily accessible monitor for loop problems. It permits diagnosis of most troubles. If it saturates to -11.5 V, insufficient gain is available to produce the required output.

The first step in the Troubleshooting Chart (see Table 4-1) that involves the PIN voltage is Step 15. To obtain -16 dBm output from the IM requires a PIN voltage of -11.5 V; since the loop is open (SA connected to IM output), the OA will produce this voltage unless it is faulty. The OA, however, must see +2.0 V at its pin 22. This voltage comes from the front panel level pot. A built-in voltage divider or an external feed through programming connector pin 22 supplies this voltage in instruments without front panel controls. If no positive voltage is available on OA pin 22, check these sources. If the voltage is normal, but no output is available, check output coax cable, connectors and R26, C23 in the OA module.

10-3-5. Module Check

After one of the three modules has been found suspect or defective, it is recommended that the module be returned to the factory for repair. In emergency situations a number of checks are detailed below, which may enable a skilled technician to locate the specific fault.

Most failures of active devices result in drastic changes of the DC voltages of the semiconductor. For this reason DC checks are always the proper first step.

Replacement of faulty components requires careful use of printed-circuit repair techniques as applicable to double-sided boards with plated-through holes.

10-3-6. OA Module Tests

Carefully remove module after releasing 6-32 screws and coax connectors below the deck. Remove cover from module. To perform DC tests, the module has to be powered, preferably through a 10 pin, card-edge connector (0.156 spacing) with: -12.4 V at pin 28, current 120 mA; +5.4 V at pin 26, current 90 mA. Ground return is pin 19.

Transistor currents in the RF part of the OA are best checked by measuring the drop across the emitter resistors.

Q	Resistor	Voltage
1	R5, R6	0.8 V
2	R9, R10	0.6 V
3	R16, R17	2.3 V
4	R28	1.3 V
5	R24	1.3 V

Deviations of over 20% are not normal. Replacement of any of the above transistors will require calibration. Part or transistor replacement in the detector amplifier part of the OA calls for recalibration of output level.

10-3-7. SO Module Tests

Check -12.4 V current with ammeter (in Yel. lead). Normal values are 180-200 mA for frequency setting of 10 MHz; and 230-250 mA for frequency setting of 150 MHz. Any significant deviation confirms some component or wiring fault, which might be detectable by careful inspection of the open module.

Unplug bottom connections, coax and feed-through clips, remove module and remove cover. Do not change any pot settings. Power module with -12.4 V through C44 and check:

1. -11.4 V regulator voltage at pin 8 - U1. Non compliance indicates trouble in regulator section around Q9 - Q11.

2. Verify mixer input levels at L4, R82 for M1 and L10, R81 for M2 to be +13 dBm. (Use RF Voltmeter). If both are off, oscillator section is suspect. If only one is off, associated amplifier section is suspect, Q1 - Q3 or Q4 - Q6. Emitter resistor voltage drops across R21, R27, R32, R55, R60, R66 are 1.7 - 2.3 V.

Generally no calibration is required after replacement of transistors and components in the amplifier and regulator sections.

10-3-8. IM Module Tests

Check -12.4 V current with ammeter (in Yel. lead). Normal value is 65 mA. Reconnect Yellow lead, remove Orange lead and apply -12.4 V through ammeter to this capacitor; normal current is 10 mA. Any significant deviation confirms a major component or wiring fault. Release coax connector and remove module after releasing the 6-32 screws; remove cover. If inspection does not provide any clues, power module with -12.4 V through C41 and measure voltage drops in the emitter resistors:

Q	Resistor	Voltage
1	R33	1.3 V
2	R27	1.3 V
3	R22	1.3 V
4	R16	1.3 V
5	R13	1.5 V

Deviations of over 20% are not normal. Replacements of transistors or components in the amplifier section Q1 - Q5 can be done without recalibration.

REPLACEABLE PARTS LIST

PC BD ASSEMBLY, SO MODULE
P/N 004.5135

Ref. Des.		Description	P/N
C1,C4,C6,C27, C29,C32	C:	Fxd cer 220 pF 10% 500 V X5F	100.1225
C2,C8,C9,C18, C26,C35,C41, C42	C:	Fxd cer.001 uF 10% 500 V X5F	100.2105
C3,C5,C7,C20, C22,C24,C28, C30,C34,C43	C:	Fxd cer 10 pF 5% 500 V NPO	100.0109
C10	C:	Fxd cer 27 pF 5% 500 V NPO	100.0279
C11	C:	Fxd cer 12 pF 5% 500 V NPO	100.0129
C12	C:	Fxd cer 33 pF 5% 500 V NPO	100.0339
C13	C:	Fxd cer 6.8 pF ± .25 pF 500 V NPO	106.9689
C14	C:	Fxd cer 15 pF 5% 500 V NPO	100.0159
C15,C36	C:	Fxd cer .01 uF +80 -20% 50 V Z5V	100.3101
C16	C:	Fxd cer 5.0 pF ± .25 pF 500 V NPO	100.9509
C17	C:	Fxd cer 1.0 pF ± .25 pF NPO	106.9109
C19,C31,C33,C37	C:	Fxd tant 6.8 uF 20% 16 V	109.5680
C21	C:	Fxd cer 3.3 pF ± .5 pF 500 V NPO	100.9338
C23	C:	Fxd cer 2.2 pF ± .5 pF 500 V NPO	100.9228
C25(P44), C38(P43), C39(P42), C40(P41), C44(P45)	C:	Fxd cer .0015 uF 500 V FD -Thru	106.2154
CR1,CR2,CR3,CR4,	CR:	Sil Zr 12 V 5% 400 mW (1N9638)	131.0121
CR5	CR:	Sil Zr 6.8 V 5% 1 W (1N3829A)	131.9681
CR6,CR7	CR:	(BB 141)	133.0141
CR8	CR:	Sil Zr 5.1 V 400 mW (1N751A)	131.9510
CR9	CR:	Sil Cmptr 75 PIV (1N4151)	132.4151
J39,J40,J46,J47	Conn:	Coax Recept	351.0010
L1	L:	Air Ind .05 uH Nom	012.1004
L2,L3	L:	Air Ind .05 uH Nom	012.1005
L4,L5,L6,L10, L11,L12	L:	Air Ind .05 uH Nom	012.1006
L7	L:	Air Ind .025 uH Nom	012.1008
L8	L:	Air Ind .030 uH Nom	012.1012
L9	L:	Air Ind .08 uH Nom	012.1011
L13	L:	Air Ind .02 uH Nom	012.1010
L14	L:	Air Ind .02 uH Nom	012.1009
M1,M2	U:	Dbl Balance Mixer	129.5000

Replaceable Parts List PC BD Assembly SO Module P/N 004.5135 Continued

Ref. Des.		Description	P/N
Q1,Q2,Q3,Q4, Q5,Q6,Q7	Q:	Sil NPN (2N5179)	134-5179
Q8	Q:	Sil NPN (2N2369)	134.2369
Q9,Q10	Q:	Sil PNP (2N3250)	136.3250
Q11	Q:	Sil NPN (2N2218)	134.2218
R1,R2,R3	R:	Var cmt 500 Ohm 10% 3/4 rect	118.1501
R4,R5,R6,R7,R8	R:	Var cmt 1.0 K Ohm 10% 3/4 rect	118.2100
R9,R10,R11,R12, R70	R:	Var cmt 2000 Ohm 10% 3/4 rect	118.2201
R13,R14,R15,R16	R:	Var cmt 5.0K 10% 3/4 rect	118.2500
R17,R19	R:	Fxd mflm 1.00 K Ohm 1% 1/10 W	111.1001
R18	R:	Fxd mflm 1.50 K Ohm 1% 1/10 W	111.1501
R20	R:	Fxd mflm 511 Ohm 1% 1/10 W	110.5111
R21,R27,R48,R49, R60,R66	R:	Fxd cflm 220 Ohm 5% 1/4 W	116.1221
R22,R28,R33,R54, R59,R65,R83	R:	Fxd cflm 1.5 K Ohm 5% 1/4 W	116.2151
R23,R30,R35,R36, R37,R38,R58,R63, R68,R69	R:	Fxd cflm 470 Ohm 5% 1/4 W	116.1471
R24,R31,R46,R47, R57,R62,R81,R82	R:	Fxd cflm 22 Ohm 5% 1/4 W	116.0221
R25,R29,R34,R43, R61,R67	R:	Fxd cflm 4.7 K Ohm 5% 1/4 W	116.2471
R26,R44,R45,R56, R73,R74,R75	R:	Fxd cflm 4.7 Ohm 5% 1/4 W	116.9471
R32,R55	R:	Fxd cflm 330 Ohm 5% 1/4 W	116.1331
R39	R:	Fxd cflm 47 Ohm 5% 1/4 W	116.0471
R40,R41,R42	R:	Fxd cflm 2.2 K Ohm 5% 1/4 W	116.2221
R50	R:	Fxd cflm 3.3 K Ohm 5% 1/4 W	116.2336
R51	R:	Fxd cflm 1.0 K Ohm 5% 1/4 W	116.2106
R52	R:	Fxd cflm 47 Ohm 5% 1/4 W	116.0476
R53	R:	Fxd cflm 470 Ohm 5% 1/4 W	116.1476
R64	R:	Fxd cflm 15 Ohm 5% 1/4 W	116.0151
R71	R:	Fxd cflm 150 Ohm 5% 1/4 W	116.1151
R72	R:	Fxd cflm 100 Ohm 5% 1/4 W	116.1101
R76	R:	Fxd cflm 2.2 Ohm 5% 1/4 W	116.9226
R77,R78,R79,R80	R:	Fxd cflm 15 K Ohm 5% 1/4 W	116.3151
U1,U2	U:	BCD-DEC Decode/Driver (74145)	122.0145

ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
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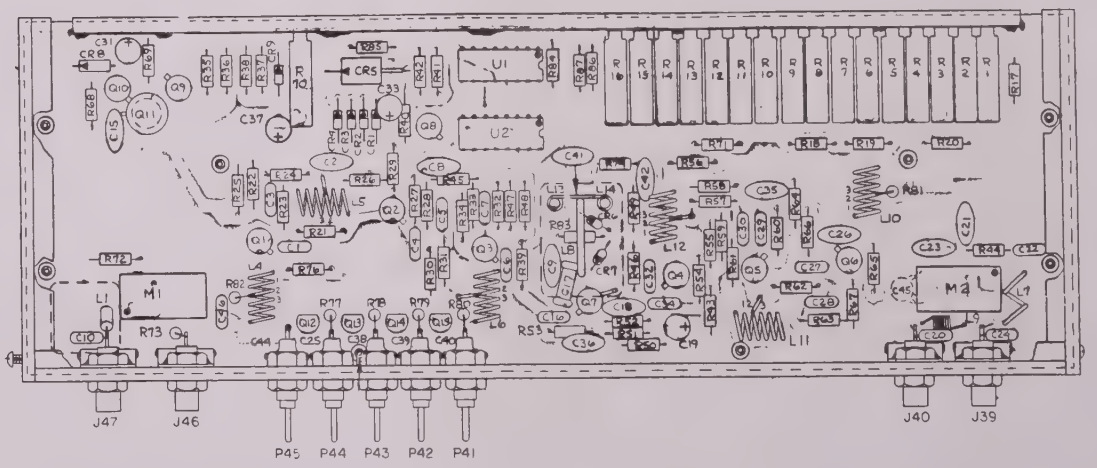

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ENG [illegible]	12/13/92	PRINTED WIRING BOARD ASSEMBLY	
MFG [illegible]	5/10/93	SO MODULE	
ISSUED			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE

.XX ±.010	.XXX ±.005	ANG ±.5°	FINISH .4

WT: ____ FSN: ____

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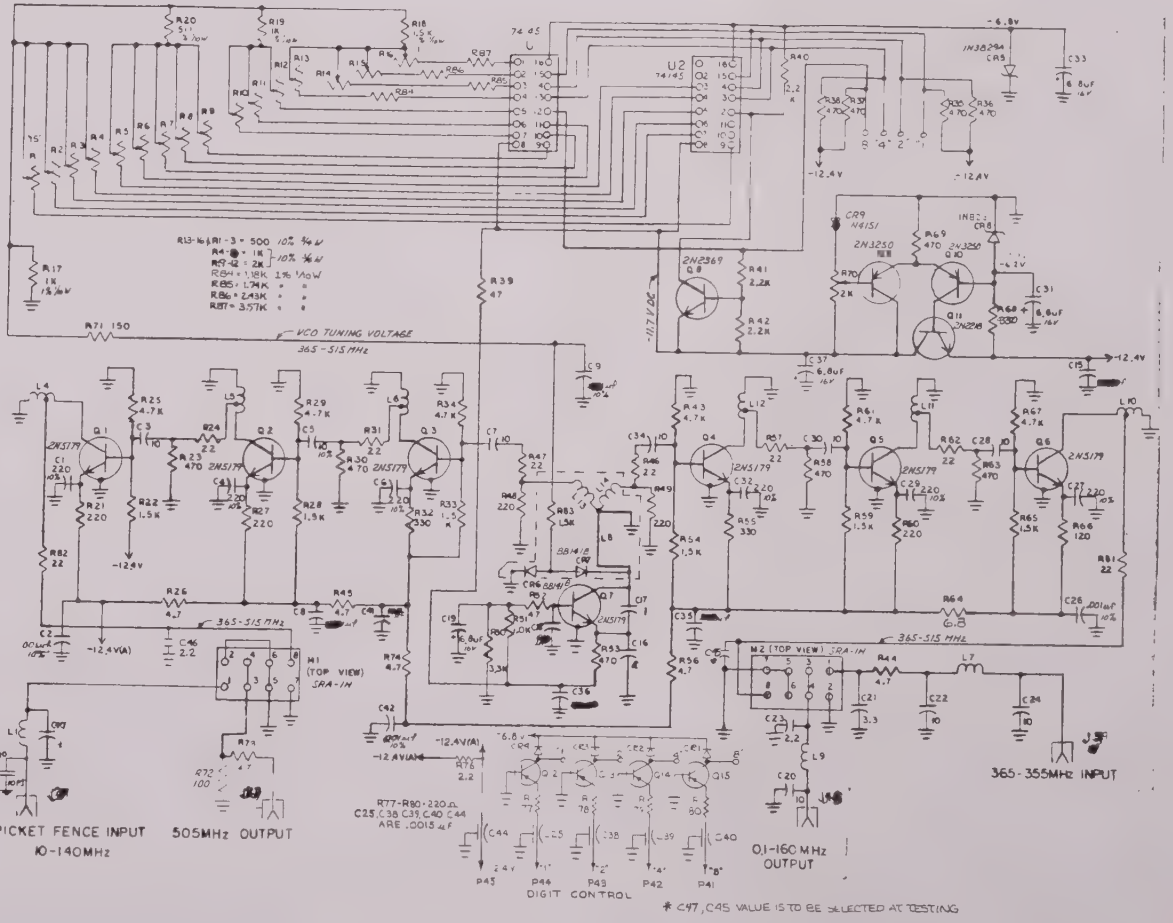
SCALE 2/1 | CAGE CODE 23338 | SHEET 1 OF 5



NOTE
1- UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE IN OHMS ¼W ±5% ALL CAPACITORS ARE 111 PF
2 - CR1 THRU CR9 ARE IN457

LTR	REC NO	CHANGED BY	APPVD BY	DATE
A				
B	208			

DRAWN BY	CR	DATE
CHECKED BY		
ENG APPVL		
MFG APPVL		

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AFTER PLATING AND TOLERANCES ARE .XXX ± .010 .XX ± .020 FRACTIONS ± 1/64 ANGLES ± 1°

ROCKLAND
Rockland Systems Corporation

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TITLE: SCHEMATIC 50 MODULE 5/30/20

SIZE D | SCALE NONE | SHEET OF | REV B

03-604-5155 REV A

REPLACEABLE PARTS LIST

PC BD ASSEMBLY, IM MODULE
P/N 004.5655

Ref. Des.		Description	P/N
C2,C4,C36	C:	Fxd cer 1.0 pF ± .25 pF 500 V NPO	106.9109
C6,C7,C8,C9, C13,C15,C18, C19,C22,C23, C26,C28,C31, C32,C35	C:	Fxd cer 220 pF 10% 500 V X5F	100.1225
C10,C25	C:	Fxd cer 10 pF 5% 500 V NPO	100.0109
C11,C42	C:	Var mica 3.5 - 13pF 5% 500 V	108.0130
C12,C17,C20,C21, C29	C:	Fxd cer 12 pF 5% 500 V NPO	100.0129
C14,C27,C34	C:	Fxd cer .01 uF +80 -20% 50 V Z5V	100.3101
C16,C24,C33	C:	Fxd cer 22 pF 5% 500 V NPO	100.0229
C30,C43	C:	Fxd cer 5.0 pF ± .25 pF 500 V NPO	100.9509
C37	C:	Fxd cer 1.5 pF ± .25 pF 500 V NPO	106.9159
C38	C:	Fxd cer 3.3 pF ± .5 pF 500 V NPO	100.9339
C39	C:	Fxd cer 2.2 pF ± .5 pF 500 V NPO	100.9229
C40,C41	C:	Fxd cer .0015 uF +50 -20% 500 V	106.2154
CR1,CR2,CR3,CR4	CR:	PIN (5082 - 3080)	133.3080
J34,J35,J38	Conn:	Coax recpt	351.0010
L1,C1,C44	Tuned Ckt Assy:	"IM" Module	012.7404
L2,C3,C45	Tuned Ckt Assy:	"IM" Module	012.7405
L3,C5,C46	Tuned Ckt Assy:	"IM" Module	012.7406
L4,L5	L:	Fxd .33 uF ± 10%	150.8332
L6	L:	Air Ind .05 uH Nom	012.1005
L7	L:	Air Ind .04 uH Nom	012.1014
L8	L:	Air Ind .04 uH Nom	012.1007
M1	U:	Dbl Balance Mixer	129.5000
Q1,Q2,Q3,Q4	Q:	Sil NPN (2SC1260)	135.1260
Q5	Q:	Sil NPN (2N5179)	134.5179

Replaceable Parts List PC BD Assembly IM Module P/N 004.5655 Continued

Ref. Des.		Description	P/N
R1,R2,R4	R:	Fxd cflm 10 K Ohm 5% 1/4 W	116.3101
R3,R7,R11,R17, R19,R28,R30	R:	Fxd cflm 2.2 K Ohm 5% 1/4 W	116.2221
R5	R:	Fxd cflm 1.5 K Ohm 5% 1/4 W	116.2151
R6,R12,R15,R21, R23,R26,R32,R34	R:	Fxd cflm 15 Ohm 5% 1/4 W	116.0151
R8,R10,R13	R:	Fxd cflm 100 Ohm 5% 1/4 W	116.1101
R9	R:	Fxd cflm 68 Ohm 5% 1/4 W	116.0681
R14,R25	R:	Fxd cflm 220 Ohm 5% 1/4 W	116.1221
R16,R22,R27,R33	R:	Fxd cflm 150 Ohm 5% 1/4 W	116.1151
R20,R24,R31,R35,R37	R:	Fxd cflm 470 Ohm 5% 1/4 W	116.1471
R29,R36	R:	Fxd cflm 4.7 Ohm 5% 1/4 W	116.9471

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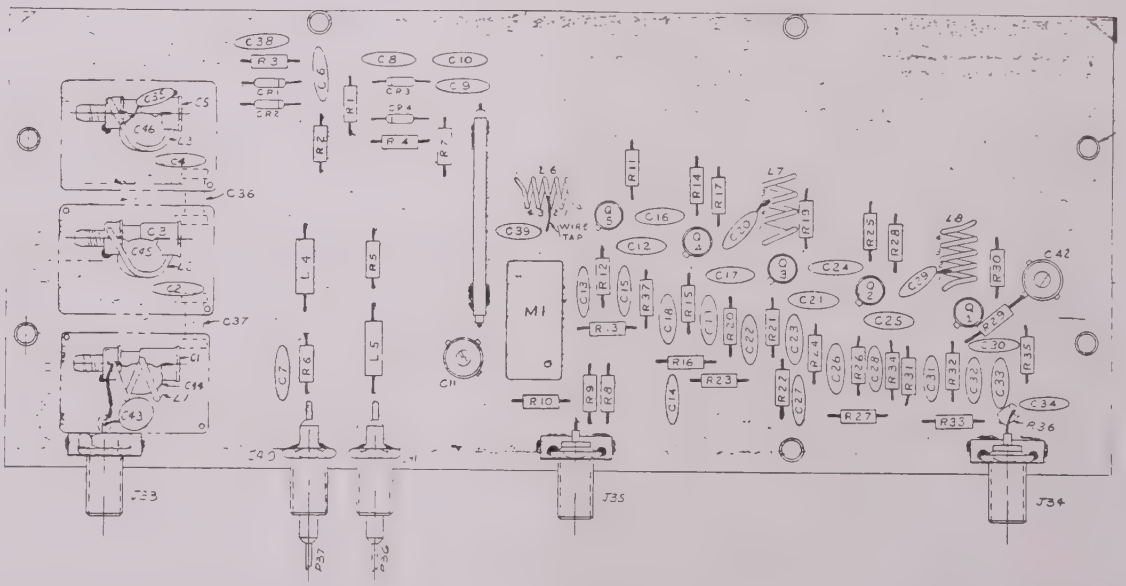
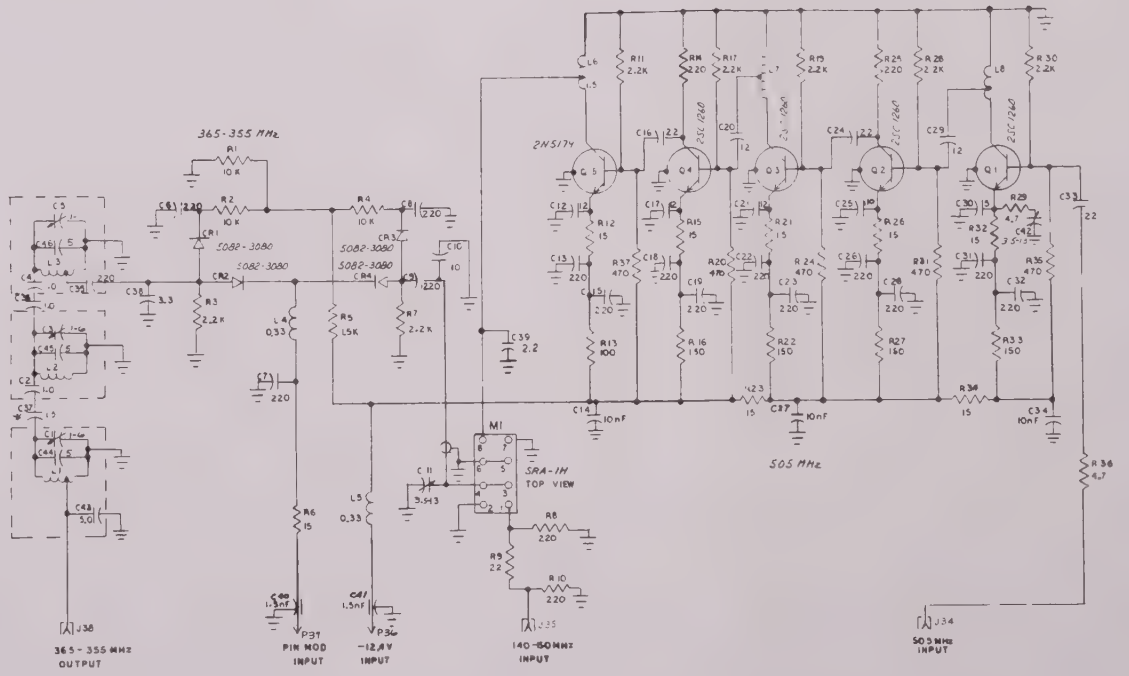
ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK ROCKLAND Wavetek Rockland, Inc.
x/x ± 1/64 | xxx ± .005 | xx ± .01 | ± 1°	DRAWN / DATE	TITLE: P.C.B ASSY 1M MODULE
MATERIAL:	CHKD	
	ENG APPR	
FINISH:	MFG APPR	
	ISSUED	SIZE: C | MODEL NO: 5130/20 | DRAWING NO: 02-004-5655 | REV: C
		SCALE | CODE IDENT: 23338 | SHEET OF



NOTES

1. UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE IN OHMS ¼W ± 5% ALL CAPACITORS IN PF
2. SELECTED AT TEST-DECREASE CAPACITY TO PROVIDE NARROWER BANDWIDTH OF TUNED CIRCUIT

LTR	ECO NO.	CHANGED BY	APPROVED BY	DATE
A	NEW RELEASE	V.A.		9-13-78
B	967	M. McMINN	V.A.	10-17-78
C	977	M. McMINN	V.A.	

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TITLE: SCHEMATIC, IM, MODULE

DWG NO. 03 JJ6-5655 REV C

SIZE D

SCALE NONE SHEET 1 OF 1

03-004-5655 C

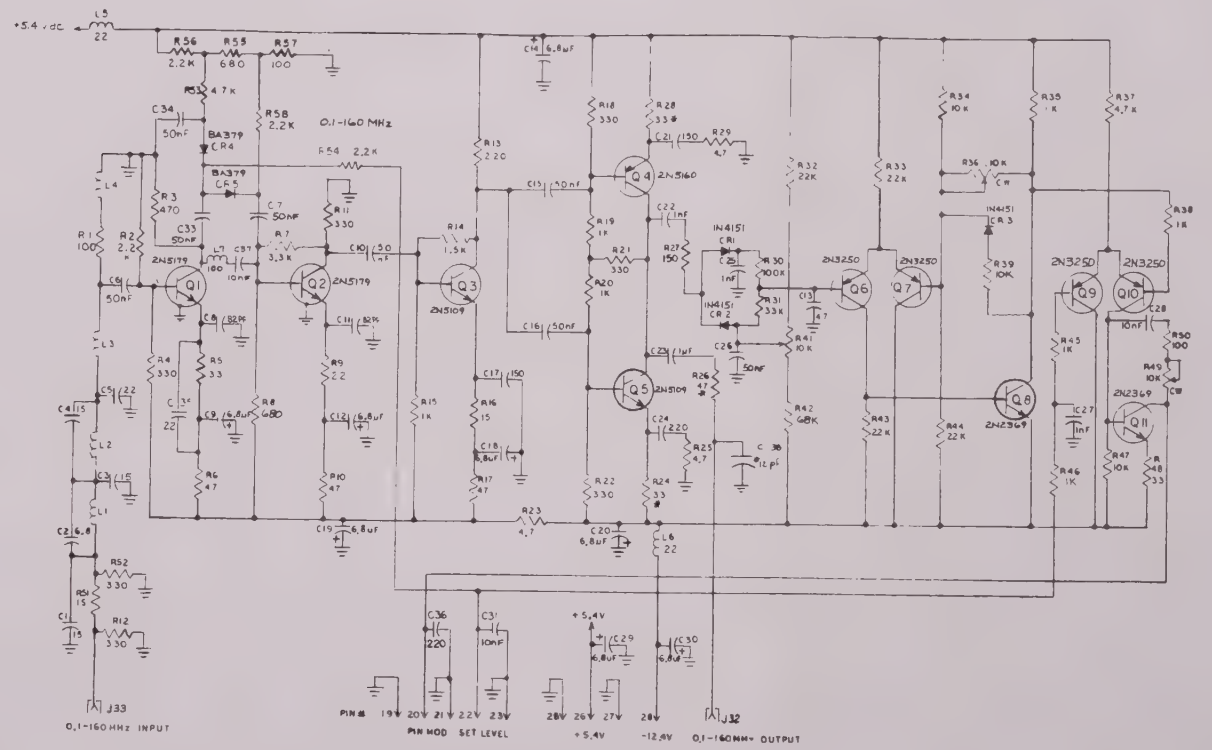
REPLACEABLE PARTS LIST

PC BD ASSEMBLY, OA MODULE
P/N 004.5660

Ref. Des.		Description	P/N
C1,C3,C4	C:	Fxd cer 15 pF 5% 500 V NPO	100.0159
C2	C:	Fxd cer 6.8 pF ± .25 pF NPO	106.9689
C5,C35	C:	Fxd cer 22 pF 5% 500 V NPO	100.0229
C6,C7,C10,C15, C16,C26,C33, C34	C:	Fxd cer .05 uF +80 -20% Z5V	100.3502
C8,C11	C:	Fxd cer 68 pF 5% 500 V N750	100.0687
C9,C12,C14,C18, C19,C20,C29, C30	C:	Fxd tant 6.8 uF 20% 16 V	109.5680
C13	C:	Fxd cer 47 pF 5% 500 V NPO	100.0479
C17,C21	C:	Fxd cer 150 pF 10% 500 V	100.1155
C22,C25,C27	C:	Fxd cer .001 uF 10% 500 V	100.2105
C23	C:	Fxd cer dp 1.0 uF 20% 50 V	106.5105
C24,C36	C:	Fxd cer 220 pF 10% 500 V X5F	100.1225
C28,C31,C37	C:	Fxd cer .01 uF +80 -20% 50 V Z5V	100.3101
CR1,CR2,CR3	CR:	Sil Cmptr 75 PIV (1N4151)	132.4151
CR4,CR5	CR:	(BA379)	133.0379
J32,J33	J:	Conn Coax Recept	351.0010
L1,L4	L:	Air Ind fxd .05 uH Nom	012.1013
L2	L:	Air Ind fxd .05 uH Nom	012.1014
L3	L:	Air Ind fxd .04 uH Nom	012.1007
L5,L6	L:	Fxd 22 uH ± 10%	150.0222
L7	L:	Fxd 100 uH ± 10%	150.1101
Q1,Q2	Q:	Sil NPN (2N5179)	134.5179
Q3,Q5	Q:	Sil NPN (2N5109)	134.5109
Q4	Q:	Sil PNP (2N5160)	136.5160
Q6,Q7,Q9,Q10	Q:	Sil PNP (2N3250)	136.3250
Q8,Q11	Q:	Sil NPN (2N2369)	134.2369

Replaceable Parts List PC BD Assembly OA Module P/N 004.5660 Continued

Ref. Des.		Description	P/N
R1,R50,R57	R:	Fxd cflm 100 Ohm 5% 1/4 W	116.1101
R2,R54,R56,R58	R:	Fxd cflm 2.2 K Ohm 5% 1/4 W	116.2221
R3	R:	Fxd cflm 470 Ohm 5% 1/4 W	116.1471
R4,R11,R12,R18, R21,R22,R52	R:	Fxd cflm 330 Ohm 5% 1/4 W	116.1331
R5,R24,R28,R48	R:	Fxd cflm 33 Ohm 5% 1/4 W	116.0331
R6,R10,R17,R26	R:	Fxd cflm 47 Ohm 5% 1/4 W	116.0471
R7	R:	Fxd cflm 3.3 K Ohm 5% 1/4 W	116.2331
R8,R55	R:	Fxd cflm 680 Ohm 5% 1/4 W	116.1681
R9	R:	Fxd cflm 22 Ohm 5% 1/4 W	116.0221
R13	R:	Fxd cflm 220 Ohm 5% 1/4 W	116.1221
R14	R:	Fxd cflm 1.5 K Ohm 5% 1/4 W	116.2151
R15,R19,R20,R35, R38,R45,R46	R:	Fxd cflm 1.0 K Ohm 5% 1/4 W	116.2101
R16,R51	R:	Fxd cflm 15 Ohm 5% 1/4 W	116.0151
R23,R25,R29	R:	Fxd cflm 4.6 Ohm 5% 1/4 W	116.9471
R27	R:	Fxd cflm 150 Ohm 5% 1/4 W	116.1151
R30	R:	Fxd cflm 100 K Ohm 5% 1/4 W	116.4101
R31	R:	Fxd cflm 33 K Ohm 5% 1/4 W	116.3331
R32,R33,R43,R44	R:	Fxd cflm 22 K Ohm 5% 1/4 W	116.3221
R34,R39,R47	R:	Fxd cflm 10 K Ohm 5% 1/4 W	116.3101
R36,R41,R49	R:	Var cmt 10 K 3/8 Sq EM	118.3103
R37,R53	R:	Fxd cflm 4.7 K Ohm 5% 1/4 W	116.2471
R42	R:	Fxd cflm 68 K Ohm 5% 1/4 W	116.3681



NOTE

1. UNLESS OTHERWISE SPECIFIED, ALL RESISTORS ARE IN OHMS, ¼W ±5%. ALL CAPACITORS ARE IN PF. ALL INDUCTORS IF SPECIFIED ARE IN UH
2. SELECTED AT TEST - R24, R26, R28, C-38 VALUES INDICATED ARE NOMINAL (*) VALUES MAY BE ADJUSTED TO PROVIDE BETTER SIGNAL OUTPUTS AND REDUCE HARMONIC DISTORTION.

LTR	ECO NO	CHANGED BY	APPVD BY	DATE
A	NEW RELEASE		KA LT	5-11-78
B	976	M MEHMAN	KA LAT	4-17-80
C	1090	FZ	KA AT	9-8-81
D	1208	SD 8-3-8		

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TITLE: SCHEMATIC, OA, MODULE

SIZE D | DRAWING NO. 03-004-5660 | REV E

SHEET 1 OF 1

03-004-5660 E

SECTION 11

OPTION 06, IEEE-STD 488/1978 INTERFACE
P/N 004.5610

11-1. INTRODUCTION: PRINCIPLES OF OPERATION

The interface functions only as a listener on the IEEE-STD 488/1978 bus. Functions that can be remotely set are synthesizer frequency and amplitude.

The interface is made through a rear panel connector that meets all the requirements of the IEEE-STD 488/1978. These signals are connected inside the synthesizer (via multipin cable) to a digital printed circuit board that plugs into a card cage. (If the interface has not been factory installed use assembly instructions on drawing 02-000-5546). The printed circuit board (henceforth called "The Interface") contains circuitry that interprets and stores data from the IEEE-STD 488/1978 bus. The interface board outputs are connected to the front panel printed circuit board of the synthesizer. The front panel board accepts remote inputs or local front panel settings to control the synthesizer.

For a through and rigorous definition of the IEEE-STD 488/1978 bus, a copy can be obtained from:

IEEE STANDARDS
347 East 47th Street
New York, New York 10017
U.S.A.

The following paragraphs will cover general principles and protocol for operating the Model 5130A in a generalized system. Specific implementation will depend on the particular details of the controller used.

11-2. DEVICE ADDRESS CODE AND MODE SELECT SWITCHES

The row of eight miniature rocker swtiches on the rear panel of the synthesizer are used to set the device address code and other operating modes.

11-2-1. Device Address Code Selection - Switches # 1 through #5

The five left-most switches allow the selection of the device address in the system. The range of addresses is from 0 to 30 (decimal) corresponding to the ASCII characters "SPACE" through " > ".

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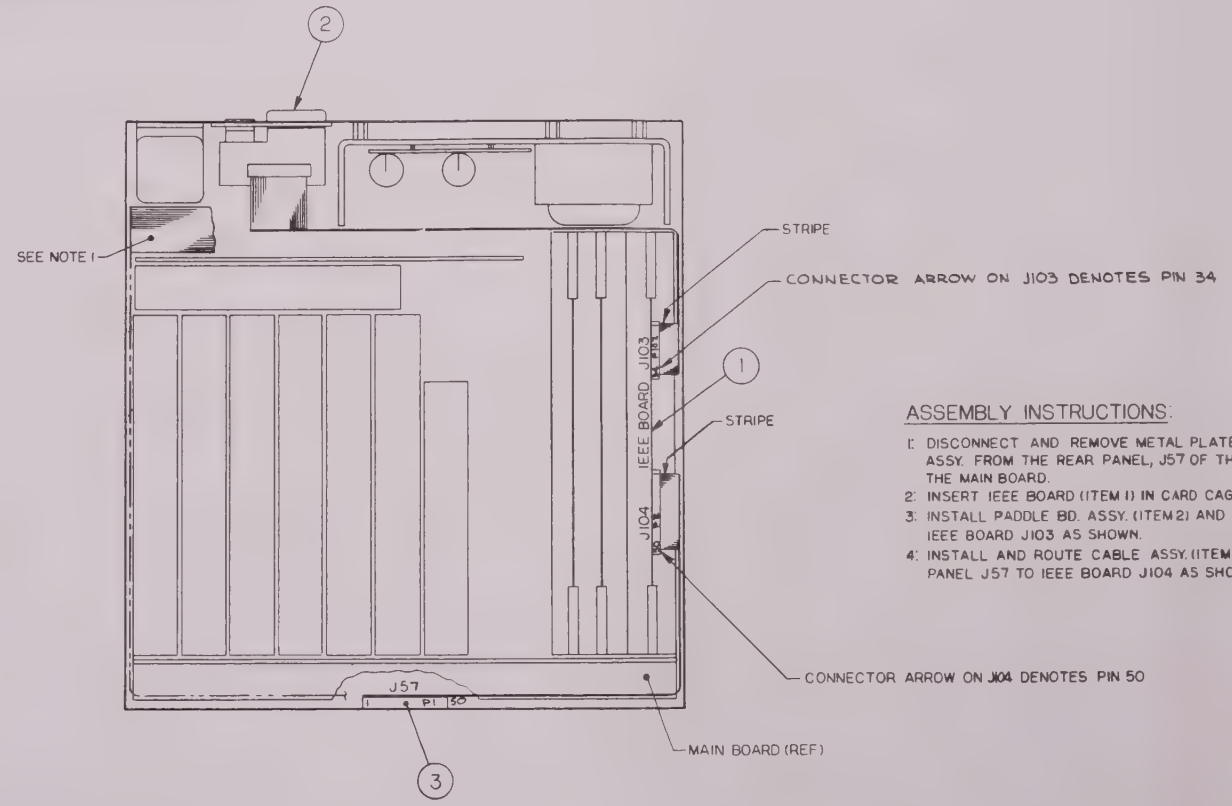
ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
	A	RELEASE		GV DSH	9/23/81
	B	1281	TC 10/23/81		



ASSEMBLY INSTRUCTIONS:

1. DISCONNECT AND REMOVE METAL PLATE AND ENTIRE CABLE ASSY. FROM THE REAR PANEL, J57 OF THE FRONT PANEL, AND THE MAIN BOARD.
2. INSERT IEEE BOARD (ITEM 1) IN CARD CAGE AS SHOWN.
3. INSTALL PADDLE BD. ASSY. (ITEM 2) AND ROUTE CABLE TO IEEE BOARD J103 AS SHOWN.
4. INSTALL AND ROUTE CABLE ASSY. (ITEM 3) FROM FRONT PANEL J57 TO IEEE BOARD J104 AS SHOWN.

FIG. 11-1

ITEM	PART NO	QTY	DESCRIPTION
1	02-004-5616	1	IEEE INTERFACE ASSY
2	02-009-9513	1	IEEE PADDLE BD ASSY
3	02-009-9514	1	CABLE ASSY IEEE/FRONT PANEL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE

X/X	.XXX	.XX	∠
± 1/64	± 005	± 01	± 1°

MATERIAL: —

FINISH. —

DO NOT SCALE DWG
REMOVE ALL BURRS
BREAK SHARP EDGES

		DATE
DRAWN M McMinn		9-16-81
CHKD		9/23/81
ENG APPR	DSH	9/23/81
MFG APPR	GV	9/23/81
ISSUED		

WAVETEK ROCKLAND — Wavetek Rockland, Inc.

TITLE: INSTALLATION OF THE IEEE-STD 488/1978 INTERFACE (OPTION-06)

SIZE	MODEL NO	DRAWING NO	REV.
C	5130/20	02-000 — 5546	B

SCALE: 1:2 | CODE IDENT 23338 | SHEET 1 OF 1

The switches have binary weights of "1", "2", "4", "8" and "16". When the top edge of the rocker is depressed, the binary weight of that switch contributes to the address. When the bottom edge of the rocker is depressed, that weight is off. For example, to set a listen address of 11 (decimal), the rocker switch pattern would be (left-to-right) on-on-off-on-off, or up-up-down-up-down.

11-2-2. Listen Always (Listen Only) Mode - Switch #6

The LISTEN ALWAYS (or LISTEN ONLY) mode allows the Model 1488A to behave as if it were always in the addressed listener mode. This eliminates the necessity for explicitly addressing the unit as a listener in simpler systems. When the LISTEN ALWAYS rocker switch is in the up (top depressed) position the LISTEN ALWAYS (LISTEN ONLY) mode is selected. When this rocker switch is down (bottom depressed), the unit must be explicitly made a listener to receive data.

11-2-3. Amplitude Control - Switch #7

The output amplitude of the synthesizer may be controlled over the range of 300 to 1000 mV RMS by means of a DC control voltage provided by the interface. In order for this amplitude control to occur, the synthesizer front panel LEVEL control must be in the detented, fully CCW position AND the rear panel AMPLITUDE rocker switch (#7) must be in the DOWN (ON) position. If either of these condition is not met, then amplitude programming is defeated.

11-2-4. Shield Ground - Switch #8

When this switch is in the up position the shield of the IEEE bus cable is electrically connected to the circuit ground of the synthesizer. When the switch is in the down position, the shield is not connected to the synthesizer.

Use of this switch may be necessary in achieving optimum noise performance in the multi-instrument system.

11-3. INITIALIZATION

After power has been applied to all devices in the system, the Controller should:

1. Send REM (Remote Enable) active (low)
2. Send IFC (Interface Clear) active (low)
3. Send IFC inactive (high)

11-4. LISTEN STATE

In order to receive data, the synthesizer must be in the LISTEN state, indicated by the green lamp on the front panel. When in the LISTEN state, the

unit will handshake and inspect all data sent over the bus. When not in the LISTEN state, the unit does not participate in the handshake and will ignore data. Two methods are available for effecting the LISTEN state:

1. Sending the LISTEN command
2. Setting the LISTEN ALWAYS switch ON

11-4-1. LISTEN Command

The LISTEN command is a universal bus command sent by the Controller containing the address of the device to be affected. After sending this command, the green LISTEN lamp on the front panel of the synthesizer should be lit.

11-4-2. LISTEN ALWAYS

If the rear panel LISTEN ALWAYS switch is set ON, then the first data handshake cycle on the bus will place the synthesizer in the LISTEN mode, lighting the green LISTEN lamp.

11-4-3. UNLISTEN STATE

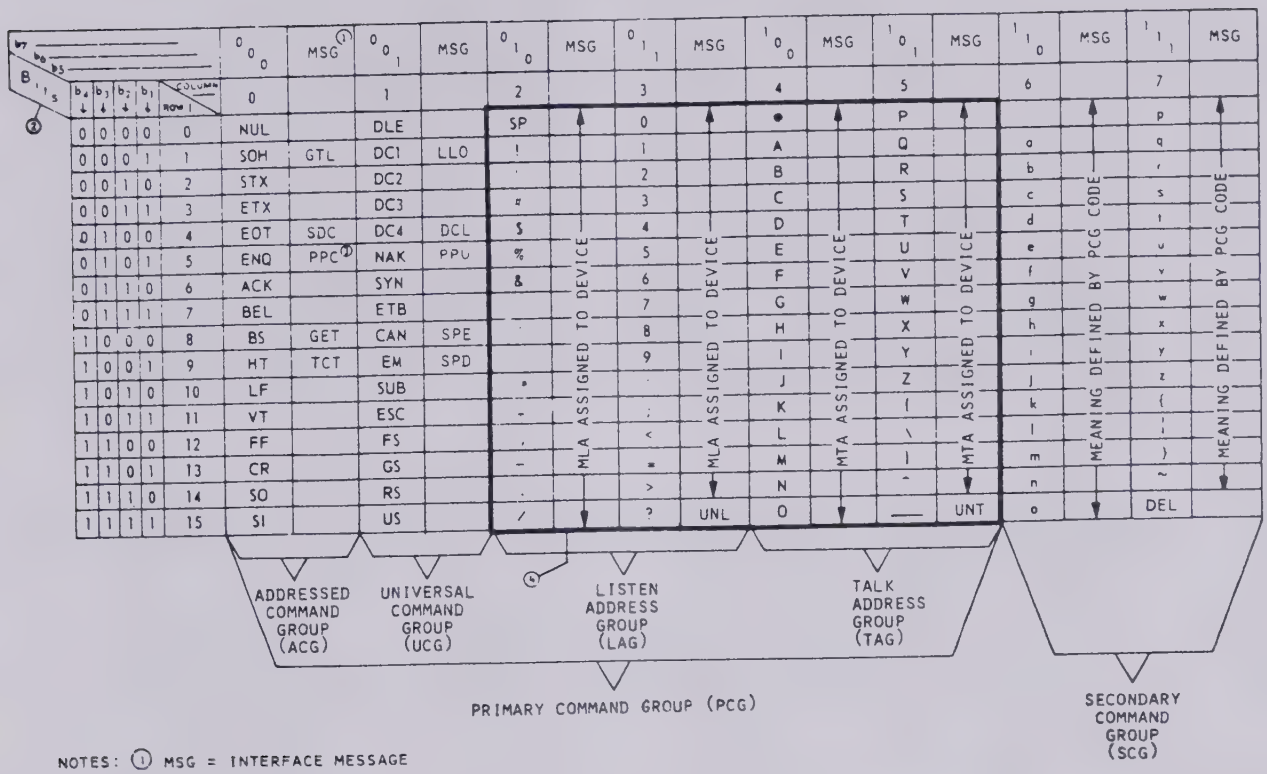
If the LISTEN ALWAYS switch is OFF, the synthesizer will leave the LISTEN state if the universal command UNLISTEN or IFC is issued. If the LISTEN ALWAYS switch is ON, the synthesizer will leave the listen state only if power is removed or IFC is issued.

11-5. SENDING DATA

All control and input data are sent in ASCII character format, which is prevalent in IEEE bus systems. A table of ASCII characters and corresponding codes is given in Fig. 11-2.

MULTILINE INTERFACE MESSAGES: ISO-7 BIT CODE REPRESENTATION

(SENT AND RECEIVED WITH ATN=1)


Multiline Interface Messages: ISO Code Representation
MLA ASSIGNED TO DEVICE
MTA ASSIGNED TO DEVICE
MEANING DEFINED BY PCG CODE
ADDRESSED COMMAND GROUP (ACG)
UNIVERSAL COMMAND GROUP (UCG)
LISTEN ADDRESS GROUP (LAG)
TALK ADDRESS GROUP (TAG)
PRIMARY COMMAND GROUP (PCG)
SECONDARY COMMAND GROUP (SCG)

NOTES: (1) MSG = INTERFACE MESSAGE
(2) b_1 = DIO1...b_7 = DIO7
(3) REQUIRES SECONDARY COMMAND
(4) DENSE SUBSET (COLUMN 2 THROUGH 5)

Reprinted from IEEE STD 488-1978 Standard Digital Interface for Programmable Instrumentation, by permission of the Institute of Electrical and Electronics Engineers, Inc.

Fig. 11-2 ASCII Characters and Codes

When in the LISTEN mode, the interface will handshake all characters sent over the bus, but only some of them are meaningful to its operation. Below is a list of such meaningful or "key" characters:

"0" through "9"	Data Value
"F"	Frequency Prefix
"A"	Amplitude Prefix
"CR"	Carriage Return for Loading

11-5-1. Frequency Commands

To enter frequency data, the character "F" must be sent followed by 12 digits for the 5130A with millihertz resolution. If "F" is sent followed by more digits than are available in the synthesizer, the high order digits will be ignored. If fewer digits are sent than are available in the synthesizer, the number is right justified with the high order bits assumed to be zero. 125 MHz would be sent as:

"F125000000000(CR)"

In order to make the entry more intelligible to the user, extra non-"key" characters may be inserted:

"Frequency = 125,000,000,000 (CR)"
"Freq: 125,000,000.000 HZ (CR)"
"F - 125 MHZ, 000 KHZ, 000 HZ, 000 MILLIHZ (CR)"

Notice that all of these entries have the same key characters.

11-5-2. Amplitude Commands

For amplitude control of the synthesizer the AMPLITUDE switch on the rear panel must be ON, and the LEVEL control on the front panel must be in the detented +3 dBm position. The interface generates a control voltage which determines the output amplitude of the synthesizer. The amplitude commands are entered by sending "A" followed by two digits specifying the amplitude of the synthesizer output in multiples of 10 mV rms. The useful range is 30 (for 300 mV rms) to 99 (for 990 mV rms). Values below 30 will cause undefined amplitude values. If more than two digits are entered only the last two will be retained.

As an example, to set the amplitude to 570 mV rms, the following could be sent:

"A57(CR)"

An "A" followed by no digits will cause an (invalid) amplitude setting of zero.

Calibration of the amplitude commands is described at the end of the Troubleshooting Section.

If the amplitude control is not required, then set the rear panel AMPLITUDE switch to the UP position (OFF) and use the front panel LEVEL control.

11-5-3. Loading Commands - "CR" and "GET"

In order to cause the entered data and the amplitude control voltage to be transferred to the synthesizer, either a "CR" (carriage return) or "GET" (group execute trigger) command is required. When either of these commands is received, the interface generates a LOAD pulse.

The termination of a digit value following a prefix character ("F" or "A") is accomplished by sending another prefix character or a "CR" or "GET" command.

The "GET" command is a universal command which is sent by the controller with ATN active. Most IEEE bus systems use this command to initiate an activity in more than one bus device simultaneously. The interface interprets the "GET" command exactly as a "CR" character, causing the loading of data into the synthesizer.

11-5-4. Combining Commands

Frequency and amplitude commands may be entered in one ASCII string followed by a "CR" or "GET" which transfers all data simultaneously to the unit. The order of commands is unimportant. If one of the commands is omitted, the last value entered will be retained (as long as power is maintained). If more than one occurrence of a command is present in a string, only the last one will be retained. The termination of a digit value following a prefix character ("F" or "A") is accomplished by sending another prefix character or a "CR" or "GET" command.

For example, to set a frequency of 45.3854 MHz in the 5130A with 1 mHz resolution and an amplitude of 630 mV rms, the following would be sent:

"F453854000000A63 (CR)" or
"A63F453854000000 (CR)"

If the frequency is to remain constant but the amplitude is to change to 720 mV rms, then send:

A 72 (CR)"

Additional non-"key" characters make the string easier for the user to issue and interpret:

"AMP = 75, FREQUENCY = 25,382,7000000 (CR)"
"FREQ: 25 MHz, 382 KHz, 700 Hz, 000 MILLIHZ (CR)"

11-6. THEORY OF OPERATION

This section will provide an abbreviated description of the IEEE Standard Digital Interface for Programmable Instrumentation otherwise referred to as

IEEE STD 488/1978, or GPIB (General Purpose Interface Bus). For a thorough and rigorous definition of this system, a copy of the standard may be obtained from:

IEEE Standards
347 East 47th Street
New York, New York 10017
U.S.A.

11-7. DESCRIPTION OF IEEE STD 488/1978 INTERFACE BUS

In general, the standard provides a physical and electrical specification to permit instruments to communicate data and control information to each other. There are three basic types of functions performed by devices connected to the bus. These functions are:

- Controller
- Talker
- Listener

Each device may possess one or more of these functions. Usually, only one device has the controller function such as a computer or programmable calculator. The controller is able to specify which of the other devices are active, control the flow of data between devices, and, in general, supervise the system.

Talkers are able to send data, and listeners are able to receive data. The controller must decide for a given transfer, which device is the talker and which device (or devices) is the listener. This is accomplished by assigning a unique device address code to each device on the bus, and by directing the controller to address and set up each device appropriately. The controller is also able to respond to interrupts and to generate trigger and clear commands.

11-7-1. Bus Lines

The following table lists the sixteen lines present in the bus system:

MNEMONIC	NAME	FUNCTION
DIO1 thru DIO8	Data Line	Bidirectional Data Lines
DAV NRFD NDAC	Data Valid Not Ready for Data Not Data Accepted	Three-Wire Handshake
IFC ATN SRQ REN EOI	Interface Clear Attention Service Request Remote Enable End or Identify	Control Lines

DIO1 thru DIO8 - Data Lines

All data, including device address codes, are transmitted over these eight lines. Usually, the data is sent as 7-bit ASCII characters, one byte or character at a time in a variable-length, serial sequence.

ATN - Attention

This control line is made active (low) by the controller when it sends device address codes over the DIO bus to change the talker/listener status of devices on the bus, or to send universal commands which must be acknowledged by all devices. When ATN is inactive (high) the data bus transfers represent input or output data.

IFC - Interface Clear

The controller makes IFC active (low) when it wishes to abort all activity on the bus and disable all devices from listening, talking or requesting service. Bus activity may not resume until IFC is returned high.

REN - Remote Enable

Remote enable, issued by the controller, must be active (low) to permit remote control operation of any device on the bus. Usually, when the line is active, front panel controls on instruments are disabled and remote inputs from the bus are accepted.

SRQ - Service Request

This line, driven by any device, indicates that some form of service is requested in the system.

EOI - End or Identify

Usually issued by a talker to designate the end of a character string, this line is also used in responding to service requests.

DAV - Data Valid

When this line is active (low) the data on the DIO bus is valid. This line is driven by the active talker.

NRFD - Not Ready for Data

This line is made active (low) by any listener before a data transfer takes place to indicate that it is not ready to accept data. Only when NONE of the listeners causes NRFD to be active can the data transfer take place. This line is read by the talker or controller which is attempting to send data.

NDAC - Not Data Accepted

Again, this line is made active (low) by any listener to extend the data transfer cycle so that it may be able to accept the data. Only when NONE of the listeners causes NDAC to be active can the data transfer by completed. This line is read by the talker or controller which is sending the data.

11-7-2. Data Handshake Cycle

Figure 11-3 shows the timing relationship involved in the three handshake control lines DAV, NRFD and NDAC.

If during this handshake cycle, ATN is active, then the handshake represents a controller command and all devices must participate in the handshake. If ATN is inactive, then only addressed listeners participate.

By holding either NRFD or NDAC active, any listener can prolong the handshake cycle allowing the slowest device to govern the data transfer rate.

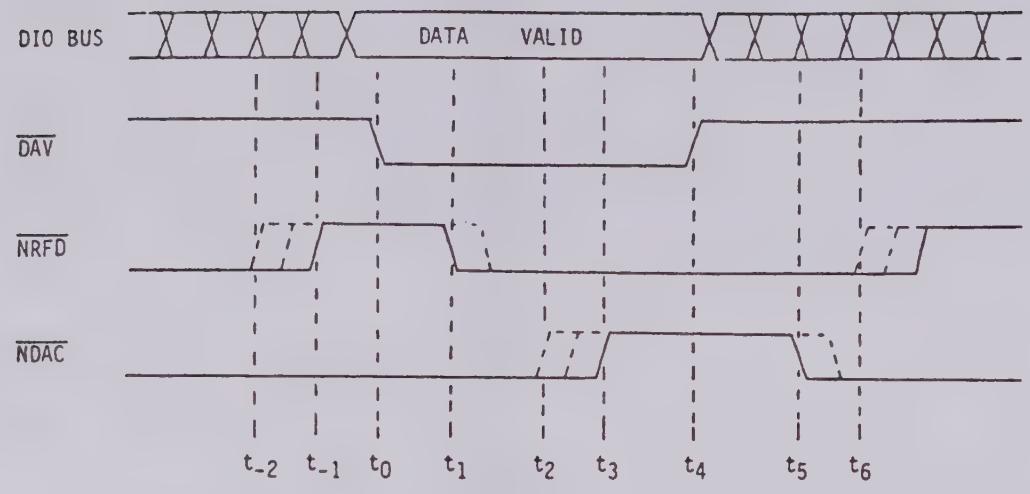
11-8. IEEE STD 488/1978 INTERFACE FUNCTIONS

The interface is a listener device in the bus system. It has no capability to send data or to issue a service request. The specific functions which it performs relative to the IEEE STD 488/1978 are:

AH 1 - Acceptor Handshake
L 1 - Basic Listener (with Listen Only capability)
DT 1 - Device Trigger

The acceptor handshake function provides for the three wire data handshake described in Section 11-7-2. The listener function is required for it to accept program data from the bus.

Listen Only (or Listen Always) is provided to allow simpler systems (where there may be only one listener) to avoid the overhead of always addressing the synthesizer as a listener for it to receive data. In addition, if the system is so simple that it does not actually need a controller, a talker with a Talk Only function and a listener with Listen Only function can constitute an operational system along.



t_{-2} First listener releases NRFD line indicating ready for data.

t_{-1} Last listener releases NRFD, letting it go inactive.

t_0 Upon sensing NRFD inactive, the talker sends data valid on the data bus and now sends DAV low indicating data is valid.

t_1 Upon sensing DAV active, each listener drives NRFD active indicating none are ready for more data.

t_2 First listener has accepted data and releases NDAC.

t_3 Last listener accepts data and releases NDAC causing it to go inactive.

t_4 Upon sensing NDAC high, the talker realizes all devices have accepted the data, takes DAV inactive, and removes data from the bus.

t_5 After sensing DAV has gone inactive, all listeners drive NDAC active.

t_6 When the first listener is ready to receive more data, it releases NRFD. This state is identical to t_{-2}, and the entire sequence repeats.

Figure 11-3 Timing Relationship for Three Handshake Control

The device trigger capability allows a predetermined function to occur simultaneously in all devices. This controller-issued command is used by the interface to cause the loading of data (previously transferred) into the synthesizer.

A block diagram of the interface is shown in Figure 11-4.

All IEEE bus connectors are made via special transceiver IC's which provide active termination, Schmitt-trigger input circuits and selectable three-state or open-collector drivers.

The control lines from the IEEE bus (IFC, REM, DAV, and ATN) enter the Control Logic section generates NDAC and NRFD bus signals and controls the entire interface.

Of the eight data lines, DIO1 through DIO8, the five least significant bits plus the five device address code bits enter the Address Comparator. Its output is used by the Control Section to recognize commands containing a device address. The seven least significant DIO bits are examined by the Control Section to recognize meaningful characters transmitted on the bus. The four least significant DIO bits enter three separate register sections for data storage.

The first register group consists of twelve four-bit registers. (The last register is actually only two bits). As frequency data is entered over the bus, the four-bit BCD words are shifted up the register, most significant digit first. Each tri-decade frequency group (mHz, Hz and KHz) is converted to a ten-bit binary number to match the programming format of the synthesizer.

The second register group is the Attenuator Register consisting of two cascaded four-bit registers storing the two attenuation digits. Conversion of these BCD digits to quasi-binary is required for the synthesizer program format.

The Control Section generates all of the timing signals which clock and clear the data registers. It consists of a FPLA (Field Programmable Logic Array) plus gates, decoders, and monostable circuits. The FPLA is programmed to recognize the appropriate codes, screen valid data, keep track of the machine state, and perform the bus handshake function.

All of the data loaded into the registers is transferred to the synthesizer when the "CR" (carriage return) or "GET" (group execute trigger) command is received. The Control Section, upon recognizing one of these commands, sends a LOAD pulse to the synthesizer causing the data to be transferred.

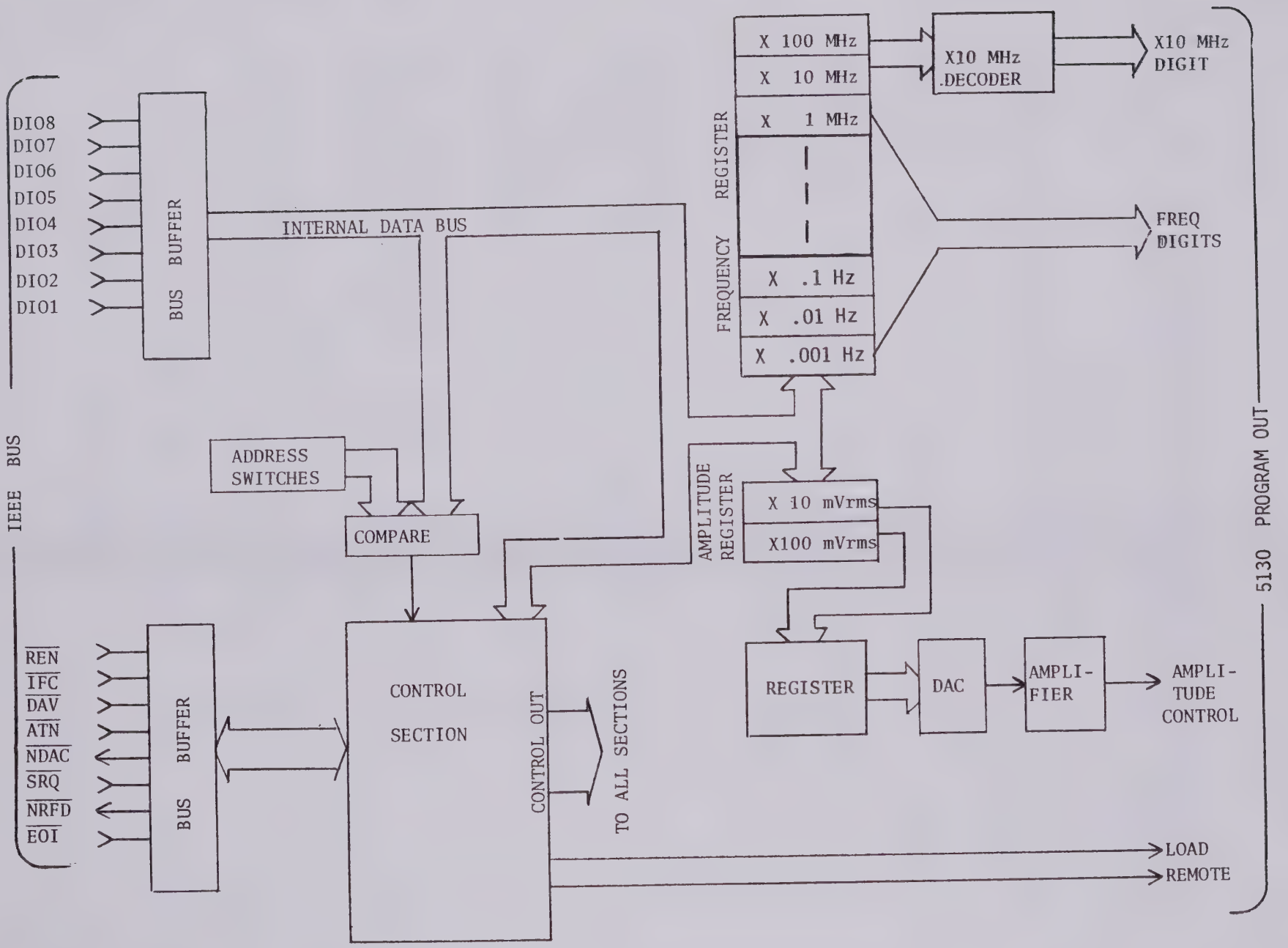


FIGURE 11.4 IEEE INTERFACE BLOCK DIAGRAM

11-9. INTRODUCTION: TROUBLESHOOTING

In the event that the bus system is not performing correctly, many functional tests may be made to help locate the cause. In general, an effort should be made to reduce both the hardware and software complexity of the system to the simplest configuration which still exhibits the problem.

Since the interface was exhaustively tested prior to shipment, the probability is low that problems encountered when first setting up the system are due to hardware failures. It is more likely that some set-up parameter, device address, or software convention is causing the problem.

Hardware failures are typically indicated only if the system has been successfully operating for some time and then fails with no system changes having been made.

11-10. CHECK LIST OF SET-UP PROBLEMS

Before attempting diagnostic tests, the following list of common set-up errors should be checked:

1. Make sure power is applied to all units connected to the bus system.

2. Check tightness of the bus cable connectors. A connector which is not secured by the captive screws may become partially disengaged from its mating socket causing intermittent or open connections.

3. Review the address code structure of the system making sure that no two devices unintentionally share the same address code. Make sure the controller is correctly identifying each device by its respective address.

11-11. DIAGNOSTIC TESTS

Problems can generally be classified as either related to the bus system operation or to the synthesizer itself. The controller is usually provided with some fault-indicating messages which can be useful in diagnosing bus problems.

11-11-1. Bus Testing

The most basic bus activity is the handshake function which is required for all universal commands and data transfers. The controller will generally indicate if there is a problem in completing the handshake. If a problem exists, the offending device can be determined by connecting devices to the bus one at a time.

The next level of activity is establishing the various devices as active listeners or talkers. The synthesizer indicates its status by the green

LISTEN lamp. Each bus device should respond appropriately to these universal commands and not interfere with each other. A unit-by-unit check of these operations will verify correct performance of these functions.

11-11-2. IEEE Interface Testing

If bus activity appears normal but data is not being loaded correctly into the synthesizer, make sure that the "CR" or "GET" command is being issued by the controller. In addition, the green REMOTE lamp on the front panel of the synthesizer must be lit during remote transfers. If not, check that the REMOTE ENABLE line on the bus is sent active by the controller.

11-12. HARDWARE TESTING

If the above tests have not uncovered the problem and troubleshooting of the hardware is required, then the information in Section 11-7 and the schematic diagram may be used to help trace the problem.

11-13. FACTORY ASSISTANCE

If the problems cannot be remedied by these procedures, factory assistance is available by calling or writing:

Application Engineering
Wavetek San Diego
9045 Balboa Avenue
San Diego, CA 92123
Phone: (619) 279-2200
TWX: (910) 335-2007

Before returning a unit to the factory for repair, authorization from Customer Service must be obtained. A written description of the problem and any related symptoms will assist the factory in making a complete and prompt repair.

11-14. CALIBRATION OF AMPLITUDE COMMANDS

Due to normal component tolerances, the relationship between the amplitude commands and the actual rms voltage value of the Model 5600 output are only nominal. Temperature, frequency setting, and amplitude value all affect this accuracy. If the nominal accuracy is not sufficient for a particular application, adjustments are provided on the inferface board to adjust these parameters. The following steps must be performed to make these adjustments:

1. Disconnect the AC line cord.

2. Open the instrument top cover.

3. Connect a RF voltmeter to the output of the synthesizer (terminated in 50 Ohms).

4. Apply power to the system and program the unit for the frequency of interest and an amplitude value of "30" (for 300 mV rms).

5. Locate the two potentiometers on the IEEE interface board, R9 and R10. R10 adjusts the DC offset of the amplitude control voltage and R9 adjusts the gain.

6. Adjust R99 (offset) for a voltmeter reading of 300 mV rms.

7. Program an amplitude of "99" (990 mV rms).

8. Adjust R10 (gain) for a voltmeter reading of 990 mV rms.

9. Program an amplitude of "30" (300 mV rms) and readjust R9 (offset) for a reading of 300 mV rms.

10. Repeat steps 7, 8, 9, 10 until no further adjustments are necessary.

REPLACEABLE PARTS LIST

P.C. ASSEMBLY 5130, IEEE STD 488/1978
P/N 004.5616

Ref.		Description	P/N
C1	C:	Fxd tant 10 uF 20% 20 V	109.6100
C2,C3,C4,C6,C7, C8,C10,C11,C12, C13,C14,C15,C16, C17,C18,C19,C22, C23,C24,C26	C:	Fxd mono 0.1 uF 50 V Z5U	100.4102
C5,C29	C:	Fxd mica dp 470 pF 10% 500 V	101.1470
C9	C:	Fxd mono .01 uF +80-20% 50 V	100.3105
C20,C21	C:	Fxd tant 10 uF 20% 50 V	109.6101
C25,C27	C:	Fxd mica dp 5 pF 10% 500 V	101.0050
C28	C:	Fxd tant 1.0 uF 20% 35 V	109.5100
CR1	CR:	Sl Lw Lk 70 PIV 200 MW (IN457)	132.0457
K1	Relay:	Reed DIP 1A w/diode 5 V	175.1505
P103	Plug:	Hdr 34 P Dil Rt Ang St Lk	352.3400
P104	Plug:	Hdr 50 P Dil Rt Ang St Lk	352.5002
Q1	Q:	P.V. Reg. 5 V (78L05)	120.0053
Q2	Q:	N.V. Reg. 5 V (79L05)	120.0054
R1	R:	Fxd cflm 2.7 K 5% 1/4W	116.2271
R2	R:	Fxd cflm 1.5 M 5% 1/4W	116.5151
R3	R:	Fxd mflm 8.25 K 1% 1/8W	111.8250
R4	R:	Fxd cflm 47 Ohm 5% 1/4W	116.0471
R5,R6	R:	Fxd mflm 4.32 K 1% 1/10W	111.4321
R7	R:	Fxd cflm 18 K 5% 1/4W	116.3181
R8	R:	Fxd cflm 20 K 5% 1/4W	116.3201
R9,R10	R:	Var cmt 5.0 K 3/9 sq em	118.2501
R11	R:	Fxd cflm 10 K 5% 1/4W	116.3101
R12	R:	Fxd cflm 470 Ohm 5% 1/4W	116.1471
R13,R14	R:	Fxd cflm 4.7 K 5% 1/4W	116.2471
R15	R:	Fxd cflm 27 K 5% 1/4W	116.3271
U2	Dac:	8 Bit (2 digit BCD)	129.1504
U3	U:	Quad 2 IN NAND Buffer (74S37)	124.7437
U4	U:	Dual Type D Flip Flop (74LS74)	125.7474
U5,U7,U8,U9,U10, U11,U18,U19,U20, U22,U23,U29	U:	Quad D Flip Flop (74LS175)	125.0110
U6	U:	4 Bit Full Adder (74LS283)	125.0130
U12	U:	Quad 2 IN OR Gate(74LS32)	125.7432
U13	U:	Lin Bifet Op Amp (TL081)	120.1016

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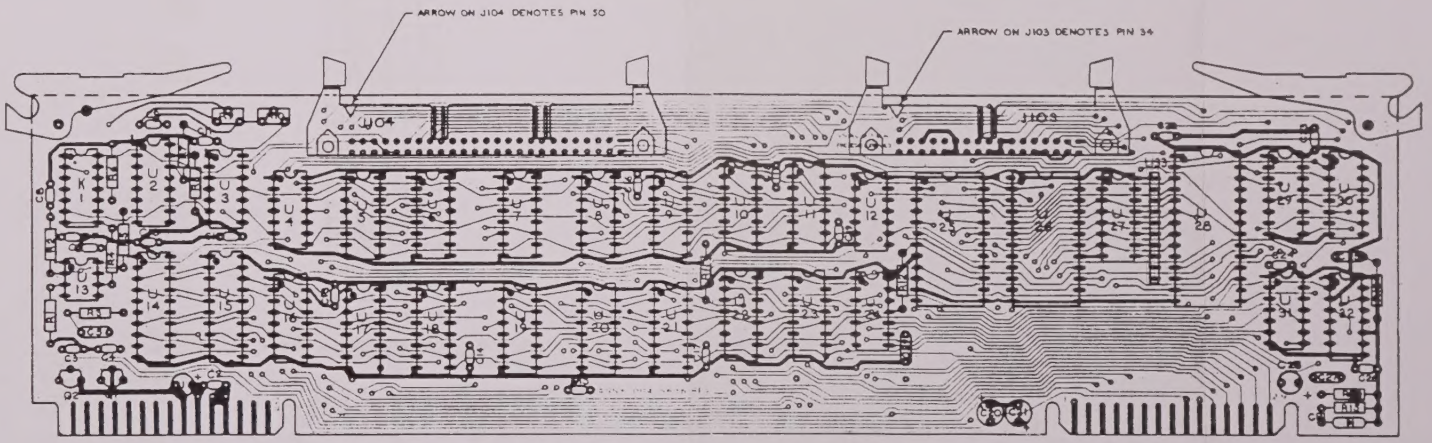

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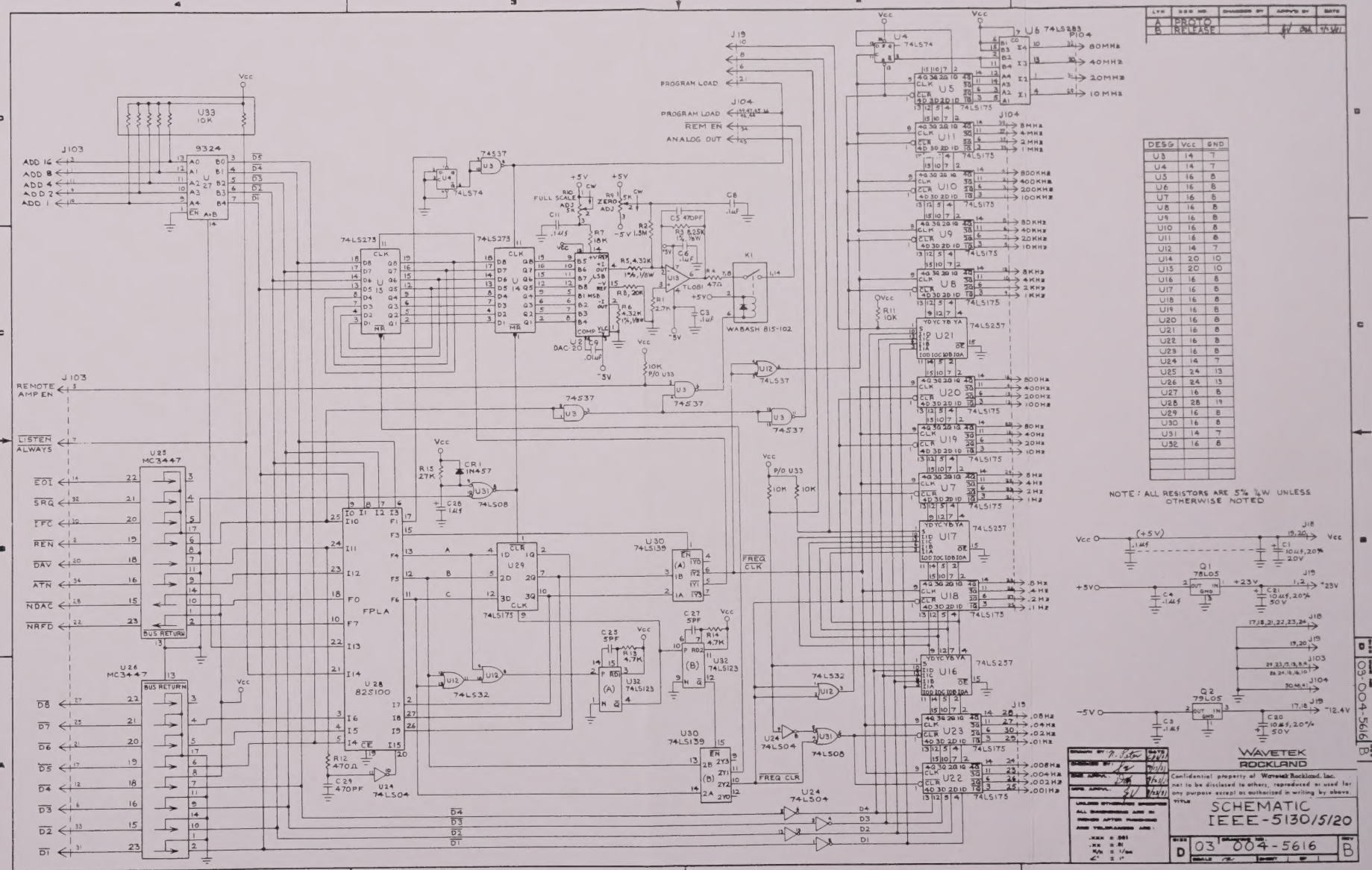

DESG	Vcc	GND
U3	14	7
U4	14	7
U5	16	8
U6	16	8
U7	16	8
U8	16	8
U9	16	8
U10	16	8
U11	16	8
U12	14	7
U14	20	10
U15	20	10
U16	16	8
U17	16	8
U18	16	8
U19	16	8
U20	16	8
U21	16	8
U22	16	8
U23	16	8
U24	14	7
U25	24	13
U26	24	13
U27	16	8
U28	28	19
U29	16	8
U30	16	8
U31	14	7
U32	16	8

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B	RELEASE			

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